S9 Maintenance Guide

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Doc. Category: Maintenance Guide
Content of This Doc.: mainly about the fault checking and hashboard tester pinpointing of Antminer S9.

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I. Maintenance Platform Requirements

1. Thermostat soldering iron at **350-400** degrees Celsius, pointed solder tip for small patches like r-c.
2. Heat gun for chip disassembly and soldering, no long-time heating in case of PCB blistering.
3. APW3 power source with **12V** and **133A Max** output to test the hashboard.
4. Multimeter, tweezer, **S9** hashboard tester (oscilloscope preferred).
5. Scaling powder, cleaning water and anhydrous alcohol; cleaning water is used to clean the residue and appearance after maintenance.
6. Tin grinder, tin stencils, and tin cream; implant tin for chips upon renewals.
7. Heat-conducting Glue, black (3461), to glue cooling fin after maintenance.

II. Maintenance Requirements:

1. Maintenance technician in possession of good electronics knowledge, 1 year+ experience and sound mastery of QFN encapsulation and soldering techniques.
2. Check more than two times after maintenance and the result of each time is OK!
3. Watch out for the techniques used, make sure of no obvious PCB deformation after changing any fittings, check for missing/open circuit/short circuit on parts.
4. Check the maintenance target and corresponding test software parameter and hashboard tester.
5. Check whether tools and testers can work properly.

III. Principle and Structure

● Principle Introduction

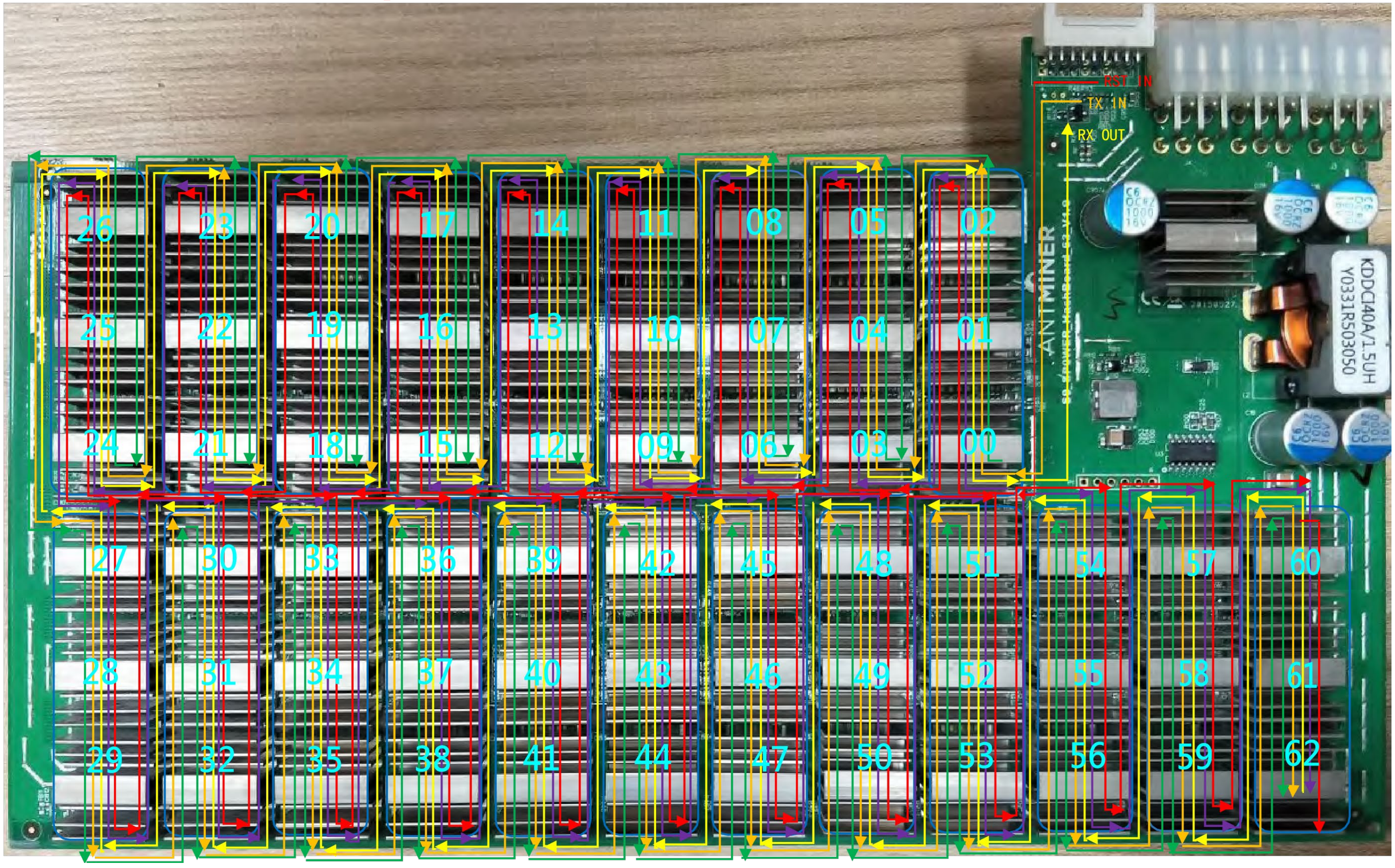
1. **S9** has **21** voltage domains connected in series, each domain has **3 BM1387**, and the entire board has **63 BM1387** chips.
2. **BM1387** chip has built-in voltage-reduction diodes, decided by designated pin of the chip.
3. **S9** has **21** voltage domains, (**S5+**: **16** voltage domains, **S7** with **54** chips: **18** voltage domains, **S7** with 45 chips: **15** voltage domains); S9 has **25M** monocrystal oscillator on the clock, connecting in series and passing on from the 1st chip to the last chip.
4. **S9** has independent small cooling fins on the front and back of each chip. **The cooling fin on the front is SMT paster and the cooling fin on the back is fixed on the back of IC by heat-conducting glue after initial test.** Upon completion of every maintenance, it has to be fixed by black heat-conducting glue (evenly distributed) on the back of IC.

Note:
In the process of maintenance, when changing board fittings or chip, in order to avoid the damage to **PCB** and chip caused by the heat from the blower gun, cooling fins near the malfunctioning part and the cooling fin on the back of **PCB** need to be removed firstly before conducting fitting changes.

PCB has test points on both sides, use the front one during maintenance in production before fitting cooling fin on the front; in product maintenance (after-sales maintenance), cooling fins are on both sides of **PCB**, locate fault through test points of **PCB**, and use specially made long and thin pen-shape meter to probe into the gaps of cooling fin for test; because the SMT small cooling fins connect the ground of each voltage domain, watch out the insulation of pen-shape meter, to avoid short circuit caused by pen-shape meter.

●Key Point Analysis:

1. Below is the signal flow diagram of S9 signal panel: (this figure takes S9 V1.9 version for example, the sequence of chips is various in different version, but the total number of chips is the same):


RST IN
TX IN
RX OUT
26
23
20
17
14
11
08
05
02
25
22
19
16
13
10
07
04
01
24
21
18
15
12
09
06
03
00
27
30
33
36
39
42
45
48
51
54
57
60
28
31
34
37
40
43
46
49
52
55
58
61
29
32
35
38
41
44
47
50
53
56
59
62
ANTMINER
KDDCI40A/1.5UH
Y0331R503050

The PCB chip sequence of S9 V1.9 version: 9 voltage domains above and 12 voltage domains below.

Fig 1. Signal Flow
This figure takes S9 V1.9 version for example

→ Green is CLK signal flow, produced by Y1 25M crystal oscillator, transmits from No. 00 chip to No. 62 chip; in standby and computing, both the votalges are 0.9V.

→ Orange is TX (CI, CO) signal flow, IO mouth pin 1 in, transmits from No. 00 to No. 62; the voltage is 0V when IO signaling wire is not plugged, and the voltage is 1.8V in computing.

← Yellow is RX (RI, RO) signal flow, returns from No. 62 to No. 00, and then returns to control panel from IO mouth pin 12; the voltage is 1.8V when IO signaling wire is not plugged, and the voltage is also 1.8V in computing.

→ Purple is B (BI, BO) signal flow, lowers electrical level from No. 00 to No. 62; the voltage is 0V when IO signaling wire is not plugged or in standby, and the singal impluse is about 0.3 in computing.

→ Red is RST singal flow, IO mouth pin 15 in, transmits from No. 00 to No. 62 chip; 0V when IO signaling wire is not plugged or in standby, and 1.8V in computing.

2. Fig 3 shows the critical circuits on the front of S9 hashboard. (Fig 3 takes S9 V4.21 for example)

① Test Points among Chips (after amplification as Fig 2):

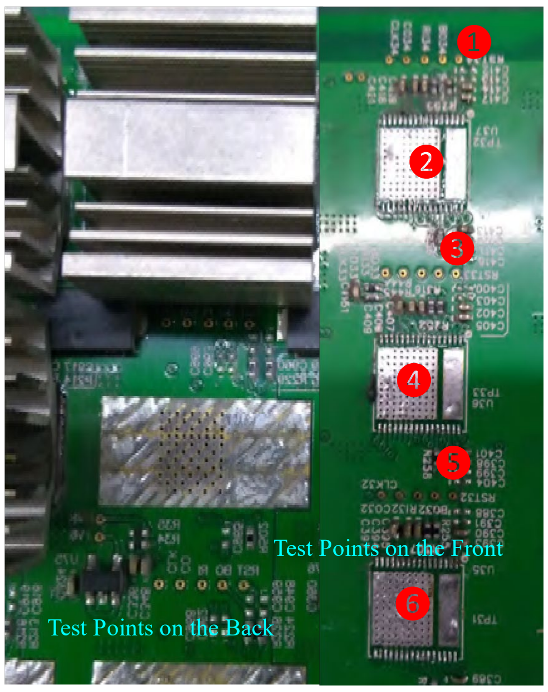


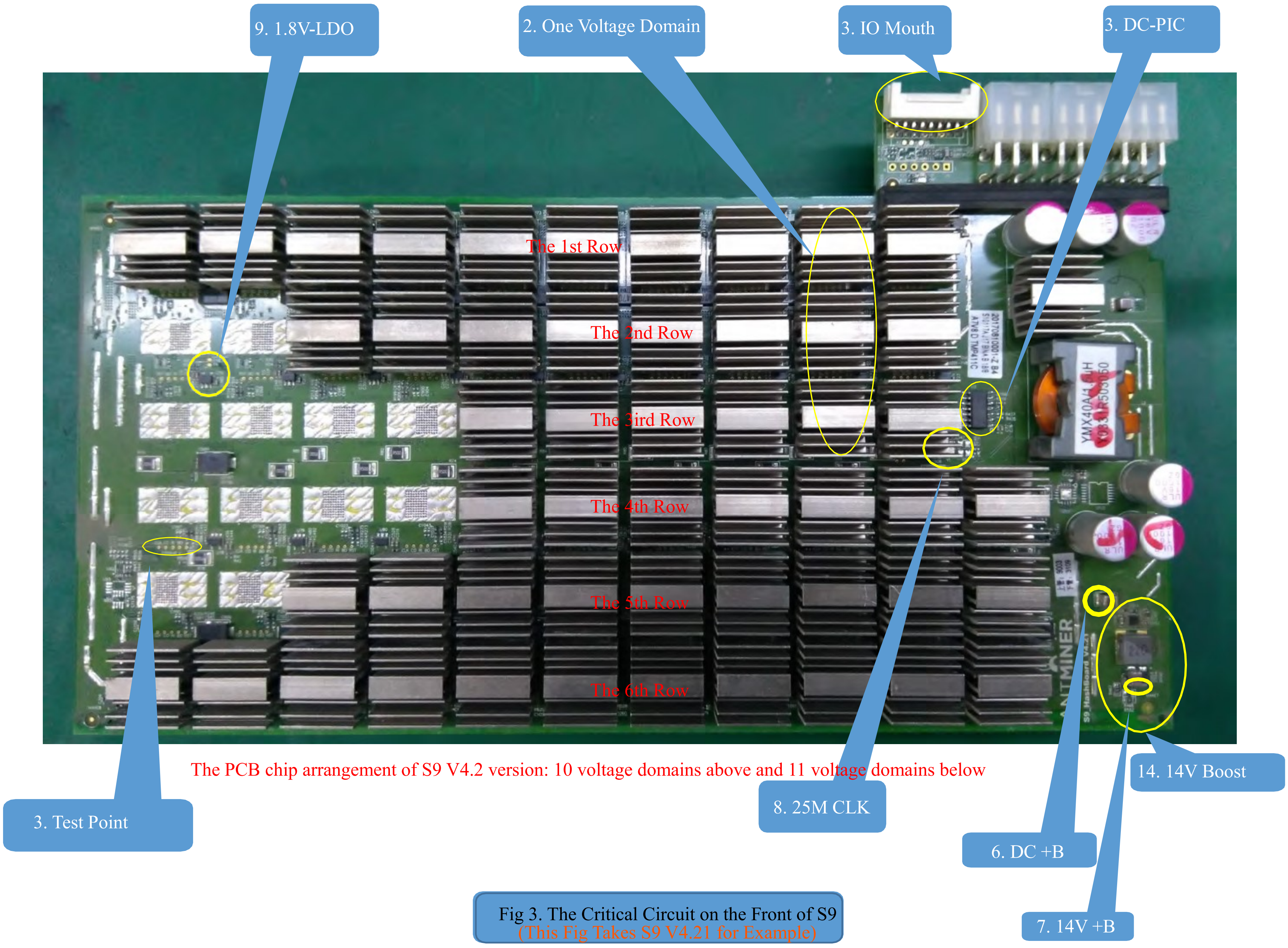
Fig 2. Test Points among Chips

In maintenance, testing the test points among chips is the most direct fault-locating method. The sequence of S9 hashboard is as the following:

The sequence of the 9 voltage domains (10 voltage domains in the upper rows in 4.2 version) of upper rows of version 1.9: RST, BO, RI (RX), CO(TX), CLK. The sequence of the 12 voltage domains (11 voltage domains in the lower rows in 4.2 version) of lower rows is reverse: CLK, CO(TX), RI(RX), BO, RST.

Fig 1 shows: RX signal transmits by the direction of 2-4-6, TX(CO) signal transmits by the direction of 6-4-2; when the RX voltage of test point 1 in Fig 2 is normal, and RX of test point 3 has no voltage or low voltage, it shows that chip 2 is poor; and when CO voltage of test point 5 in Fig 2 is normal, and CO of test point 3 has no voltage or low voltage, it shows that chip 4 is poor.

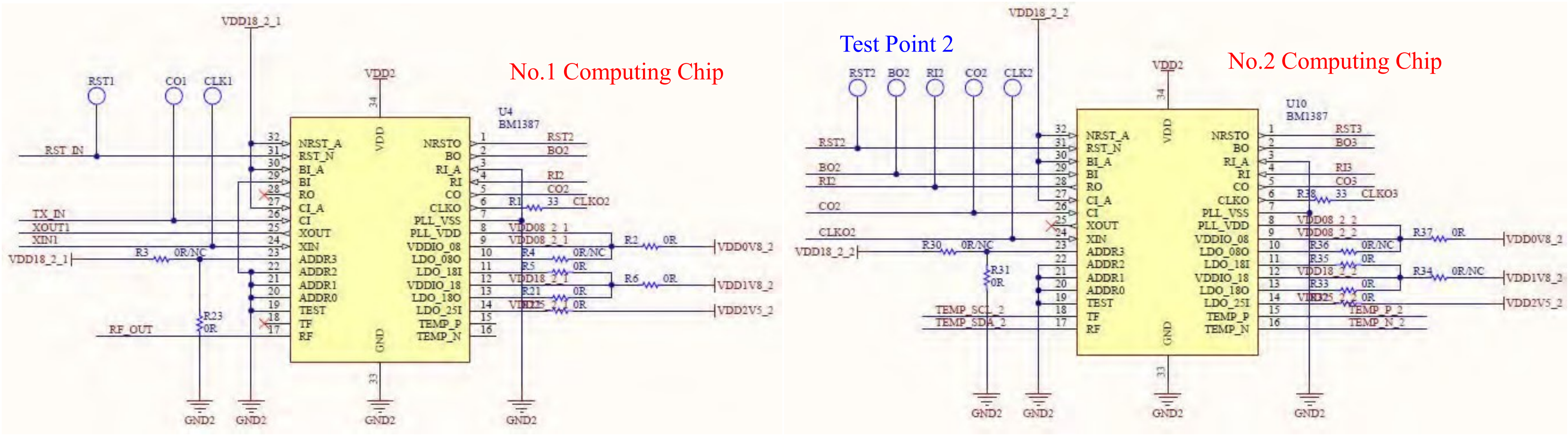
The voltages and resistances of the 5 test points in the1st row and 6th row are exactly the same theoretically, and the voltages and resistances of the five test points in the middle four rows from the 2nd to the 5th are exactly the same theoretically
In the 1st and 6th row, CLK voltage is 0.4-0.9V, CO 1.6-1.8V, RI 2.1-2.2V, BO 0V, RST 1.6-1.8V
In the 1st and 6th row, CLK resistance is 780, CO 570, RI 570, BO 570, RST 430 (in some versions, RST resistance is 570)
From the 2nd row to 5th row, CLK voltage is 0.9V, CO 1.6-1.8V, RI 1.6-1.8V, BO 0V, RST 1.6-1.8V
From the 2nd row to 5th row, CLK resistance is 570, CO 520, RI 520, BO 520, RST 420(in some versions, RST resistance is 520)



The PCB chip arrangement of S9 V4.2 version: 10 voltage domains above and 11 voltage domains below

Fig 3. The Critical Circuit on the Front of S9
(This Fig Takes S9 V4.21 for Example)

② Voltage Domain: the entire board has 21 voltage domains, and each domain has 3 chips. The 3 chips in the same voltage domain are in associated power supply, and then connect other voltage domains in series. The circuit structure is as below Fig 4:


No.1 Computing Chip
VDD18_2_1
RST1
CO1
CLK1
VDD2
U4
BM1387
RST_IN
TX_IN
XOUT1
XIN1
VDD18_2_1
R3
0R/NC
RF_OUT
R23
0R
RST2
BO2
RI2
CO2
R1
33
CLKO2
VDD08_2_1
R2
0R
R4
0R/NC
R5
0R
VDD18_2_1
R6
0R
R21
0R
R22
0R
VDD0V8_2
VDD1V8_2
VDD2V5_2
GND2
Test Point 2
No.2 Computing Chip
VDD18_2_2
RST2
BO2
RI2
CO2
CLK2
VDD2
U10
BM1387
CLKO2
VDD18_2_2
R30
0R/NC
R31
0R
TEMP_SCL_2
TEMP_SDA_2
RST3
BO3
RI3
CO3
R38
33
CLKO3
VDD08_2_2
R37
0R
R36
0R/NC
R35
0R
VDD18_2_2
R34
0R/NC
R33
0R
R32
0R
TEMP_P_2
TEMP_N_2
VDD0V8_2
VDD1V8_2
VDD2V5_2
GND2

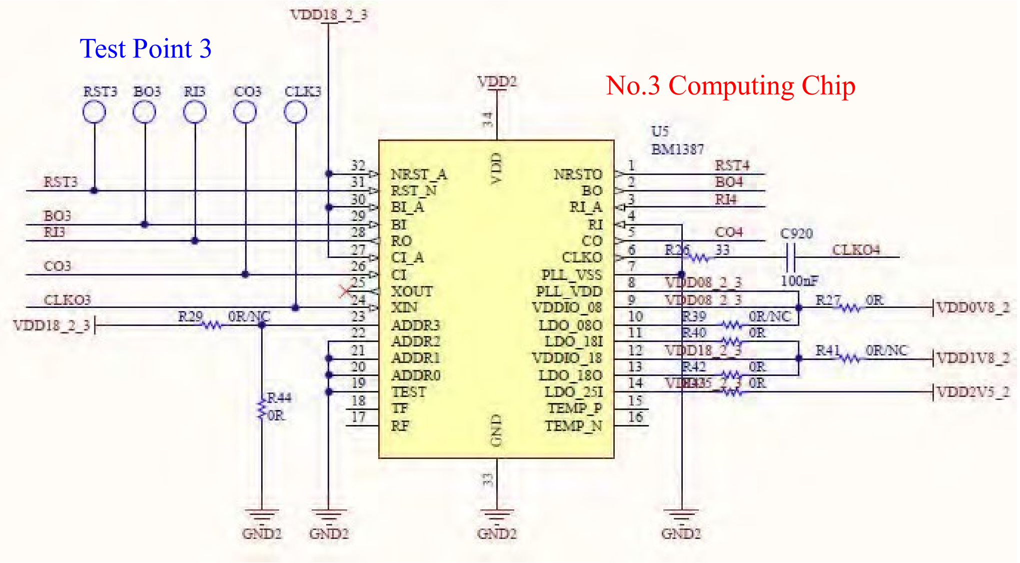

Test Point 3
No.3 Computing Chip
VDD18_2_3
RST3
BO3
RI3
CO3
CLK3
VDD2
U5
BM1387
CLKO3
VDD18_2_3
R29
0R/NC
R44
0R
RST4
BO4
RI4
CO4
C920
100nF
R26
33
CLKO4
VDD08_2_3
R27
0R
R39
0R/NC
R40
0R
VDD18_2_3
R41
0R/NC
R42
0R
R43
0R
VDD0V8_2
VDD1V8_2
VDD2V5_2
GND2

Fig 4. The Critical Circuits on the Front of S9 Hashboard

Note: S9 hashboard has different versions and they are not exactly the same. With regard to LDO-1.8V power supply of each voltage domain in early version, the 3 chips of each voltage domain are powered by independent external LDO power supply chip; and the power supply changes to chip internal power supply (chip BM1387 has LDO power supply circuit with 2.5V input and 1.8V output) in later version. Except for the last 5 voltage domains are powered by 14V booster voltage and external LDO, other chips are all powered by the LDO 1.8V of chip itself, and PLL-0.8V is from the voltage division of divider resistance from the LDO-1.8V of the 1st chip of each voltage domain (later version).

Principle Analysis of Voltage Domain Single Chip (see below Fig 5 and Fig 6):

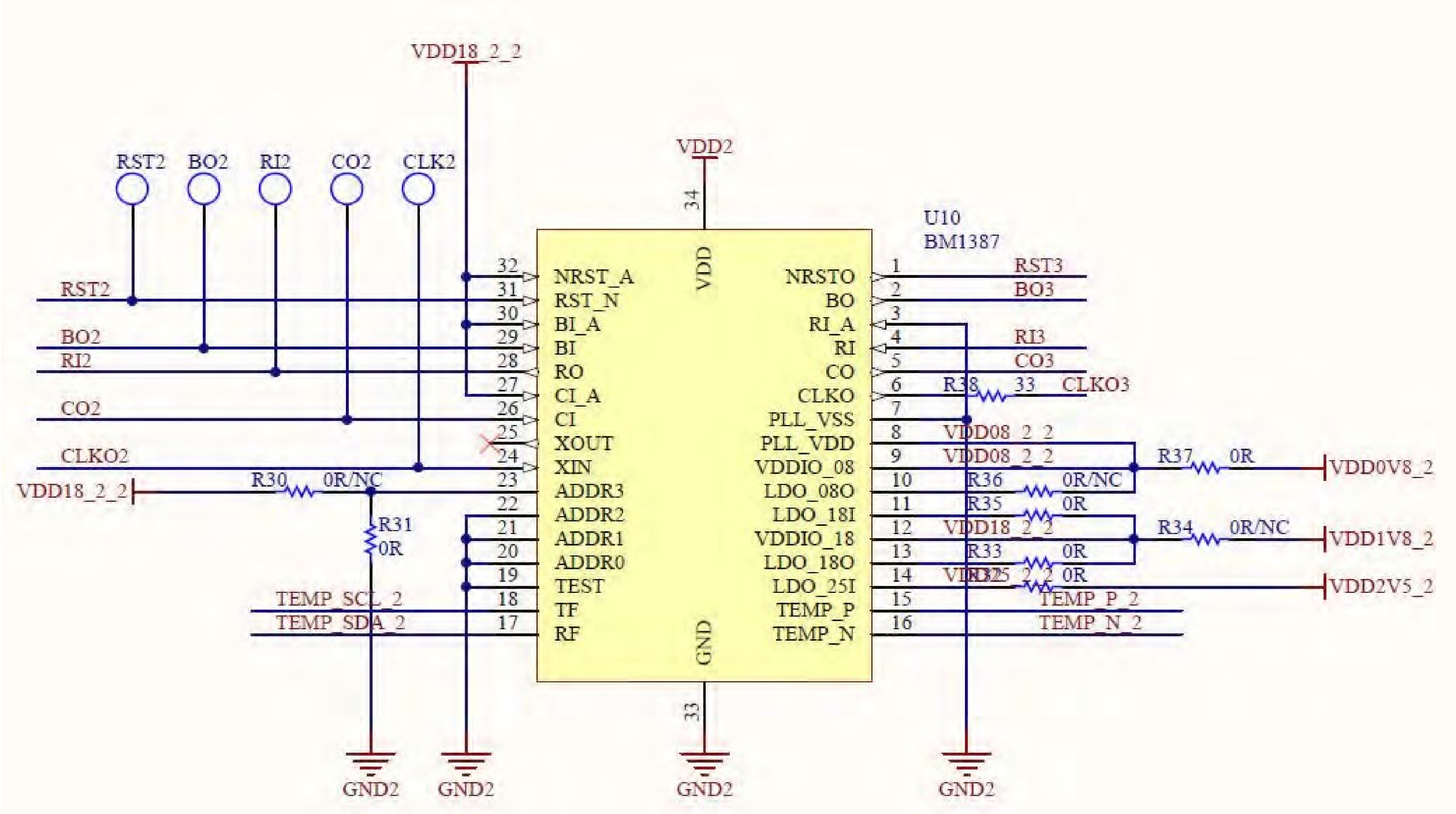

VDD18_2_2
RST2
BO2
RI2
CO2
CLK2
VDD2
34
U10
BM1387
RST2
BO2
RI2
CO2
CLKO2
VDD18_2_2
R30
0R/NC
R31
0R
TEMP_SCL_2
TEMP_SDA_2
32 NRST_A
31 RST_N
30 BI_A
29 BI
28 RO
27 CI_A
26 CI
25 XOUT
24 XIN
23 ADDR3
22 ADDR2
21 ADDR1
20 ADDR0
19 TEST
18 TF
17 RF
VDD
GND
33
NRSTO 1
BO 2
RI_A 3
RI 4
CO 5
CLKO 6
PLL_VSS 7
PLL_VDD 8
VDDIO_08 9
LDO_08O 10
LDO_18I 11
VDDIO_18 12
LDO_18O 13
LDO_25I 14
TEMP_P 15
TEMP_N 16
RST3
BO3
RI3
CO3
R38
33
CLKO3
VDD08_2_2
VDD08_2_2
R37
0R
VDD0V8_2
R36
0R/NC
R35
0R
VDD18_2_2
R34
0R/NC
VDD1V8_2
R33
0R
R32
0R
VDD2V5_2
TEMP_P_2
TEMP_N_2
GND2
GND2
GND2
GND2

Fig 5. BM1387 Circuit

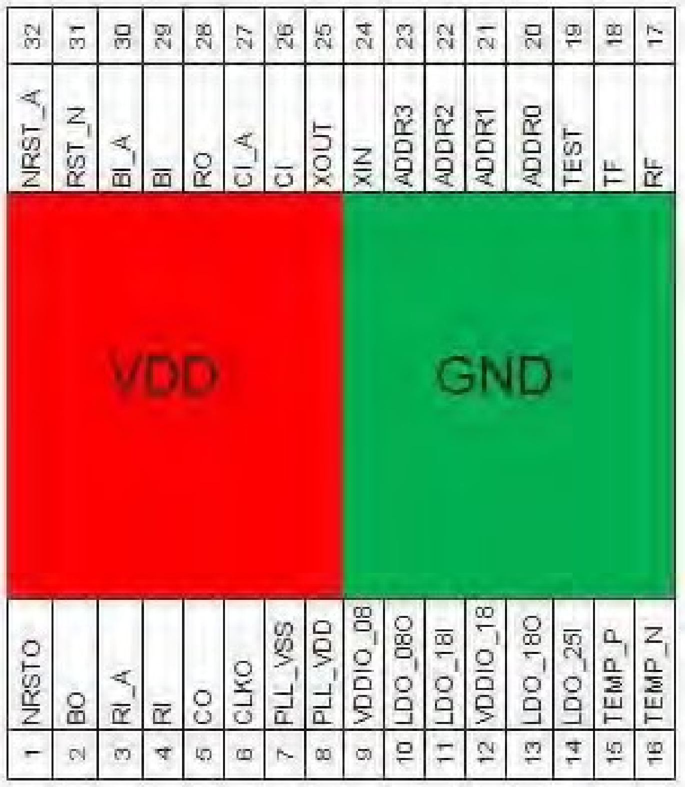

32 NRST_A
31 RST_N
30 BI_A
29 BI
28 RO
27 CI_A
26 CI
25 XOUT
24 XIN
23 ADDR3
22 ADDR2
21 ADDR1
20 ADDR0
19 TEST
18 TF
17 RF
VDD
GND
1 NRSTO
2 BO
3 RI_A
4 RI
5 CO
6 CLKO
7 PLL_VSS
8 PLL_VDD
9 VDDIO_08
10 LDO_08O
11 LDO_18I
12 VDDIO_18
13 LDO_18O
14 LDO_25I
15 TEMP_P
16 TEMP_N

Fig 6. BM1387 Chip Pins

Signal Description

	Name	I/O	Active Level	Description
1	NRSTO	O	L	Output to the chip of next level, for the loop
2	BO	O	H	Respond Busy Output
3	RI_A	I	N/A	Auxiliary Respond Input, add diode and pulldown
4	RI	I	N/A	Respond Input. Schmitt input and internal pullup
5	CO	O	N/A	Command Output
6	CLKO	O	N/A	Clock output to the chip of next level, for the loop. Pin drive current: 16A
7	PLL_VSS			PLL ground
8	PLL_VDD			PLL power (0.8V), PLL digital and analog share the same supply
9	VDDIO_08			IO VDD pre-drive, 0.8v
10	LDO_08O			LDO 0.8v output, for PLL and IO pre-drive
11	LDO_18I			LDO power input voltage range: 1.62v ~ 1.98v
12	VDDIO_18			IO VDD post-drive, 1.8v
13	LDO_18O			LDO 1.8v output for IO
14	LDO_25I			LDO power input voltage range: 2.2v ~ 2.6v
15	TEMP_P			Temperature diode positive output, analog IO. Should be floating when no use.
16	TEMP_N			Temperature diode negative output, analog IO. Should be floating when no use.
17	RF	O		Function 1: RO open drain output. Function 2: SDA0.
18	TF	O		Function 1: Respond Tx Flag. Function 2: SCL0.
19	TEST	I	N/A	Internal pull down. 0: Normal mode 1: Test mode
20	ADDR [0:0]	I		Address Input. Internal pullup
21	ADDR [1:0]	I		
22	ADDR [2:0]	I		
23	ADDR [3:0]	I		
24	XIN	I	N/A	Oscillator input
25	XOUT	O	N/A	Oscillator output

26	CI	I	N/A	Command Input. Schmitt input.
27	CI_A	I	N/A	Auxiliary Command Input, add diode and pullup
28	RO	O	N/A	Respond Output
29	BI	I	H	Respond Busy Input
30	BI_A	I	H	Auxiliary Respond Busy Input, add diode and pullup
31	RST_N	I	L	Reset signal
32	NRST_A	I	L	Auxiliary Reset signal, add diode and pullup

● The above is the function of each pin of BM1387 chip.

In maintenance, mainly test the ten test points on the front and back of chip (front and back have 5 respectively: CLK, CO, RI, BO, RST); CORE voltage; LDO-1.8V, PLL-0.8V; DC-DC output, and booster voltage 14V.

Test Methods:

❶ When IO wire is not plugged and only 12V is plugged: DC-DC output is 9V or so, and booster voltage output is about 14V. Among test points, CLK must be 0.9V, RI must be 1.8V, and the voltage of others must be 0V;

❷ When IO wire is plugged but test key is not pressed, DC-DC and booster voltage have no voltage output; when tool test key is pressed, PIC begins to work. At that moment, DC-DC outputs the voltage set up by PIC tool test program; booster voltage begins to work. Then tool outputs WORK and returns NONC after computing. This moment the normal voltage of each test point should be:

CLK > 0.9V

CO > 1.6-1.8V. When tool just sends WORK, CO is negative polarity, so DC level will be lowered and the transient voltage is about 1.5V.

RI > 1.6-1.8V. In computing, anomaly voltage or low voltage will cause hashboard anomaly or zero hash rate.

BO > 0V when there is no computing, and 0.1-0.3V impulse beat in computing.

RST > 1.8V. Every time when pressing tool test key, output reset signal again. When any test point status or voltage is abnormal, infer fault point according to the signal flow of test point.

●It can be seen from above list:

CLK signal: Pin **24** in, Pin **6** out, when crossing domains, Pin **6** out, via a 100NF capacitor, enters Pin **24** of the next chip.
TX signal: Pin **26** or **27 (crossing domain)** in, Pin **5** out;
RX signal: Pin **4** returns, Pin **28** out;
BO Signal: Pin **29** or **30 (crossing domain)** in, Pin **2** out;
RST Signal: Pin **31**or **32 (crossing domain)** in, Pin **1** out.

As shown in below Fig 7: it is able to detect each signal voltage of chip, including CORE voltage, LDO-1.8O, LDO-1.8I, PLL-0.8, LDO-2.5I, etc.
CORE: 0.4V— generally the chip CORE short circuit of this voltage domain will cause this voltage anomaly.
LDO-1.8: 1.8V— LDO-1.8O or LDO-1.8I short circuit or open circuit of this chip will cause this voltage anomaly.
PLL-0.8: 0.8V— PLL-08 power supply short circuit or LDO-1.8 anomaly of a chip of this voltage domain will cause this voltage anomaly.
LDO-2.5I: 2.5V— LDO-2.5I short circuit or open circuit of this chip will cause this voltage anomaly.

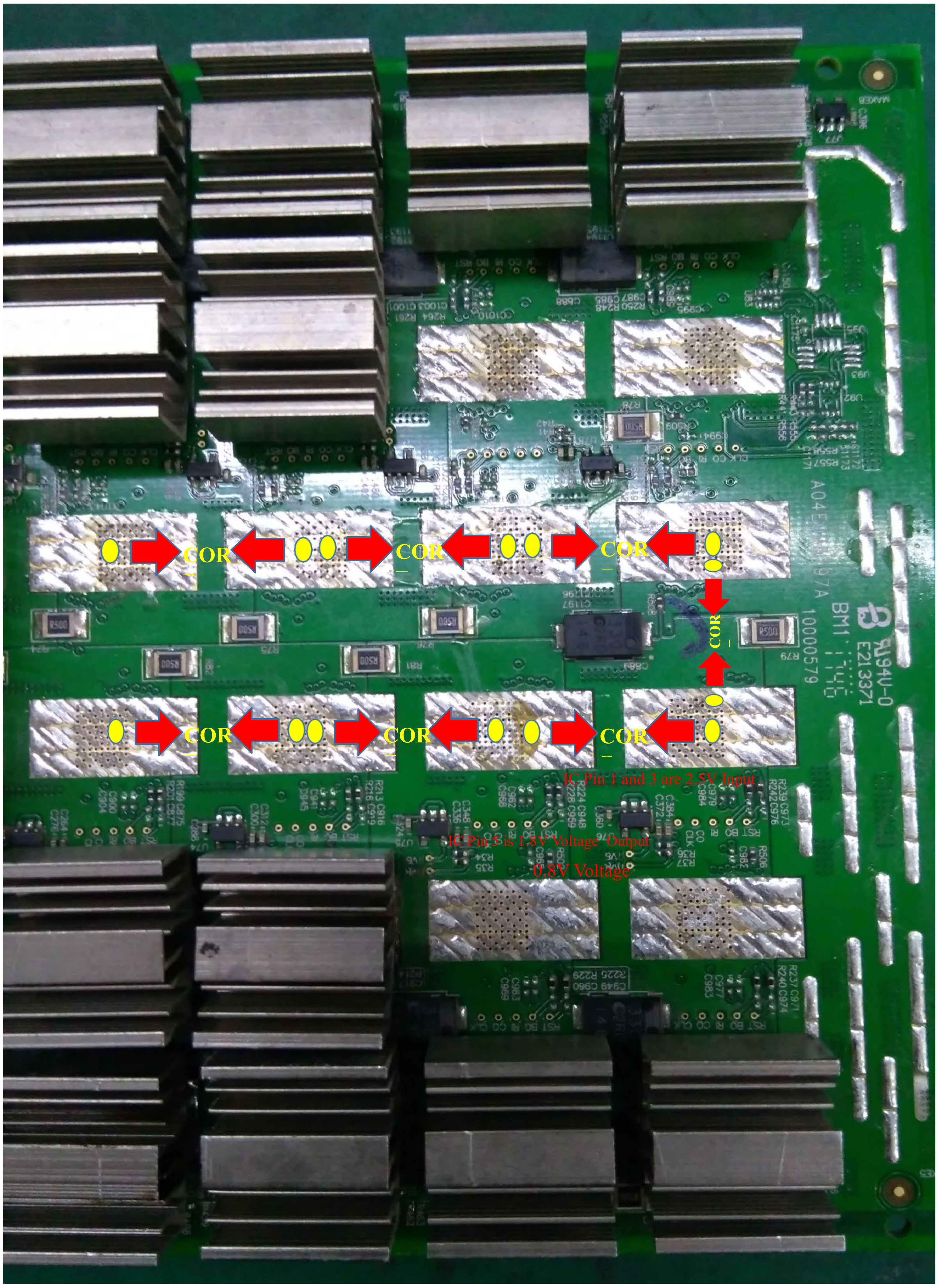

COR
COR
COR
COR
COR
COR
COR
IC Pin 1 and 3 are 2.5V Input
IC Pin 5 is 1.8V Voltage Output
0.8V Voltage

Fig 7. Test Points around Chip and Each Voltage

❸ Determine the operation status of hashboard, computing power of chip, temperature sensing, etc. according to the print window information of tool.

3. IO Mouth: IO is composed of 2X9 pitch 2.0 PHSD 90° in-line double row. The definition of each pin as below Fig 8:

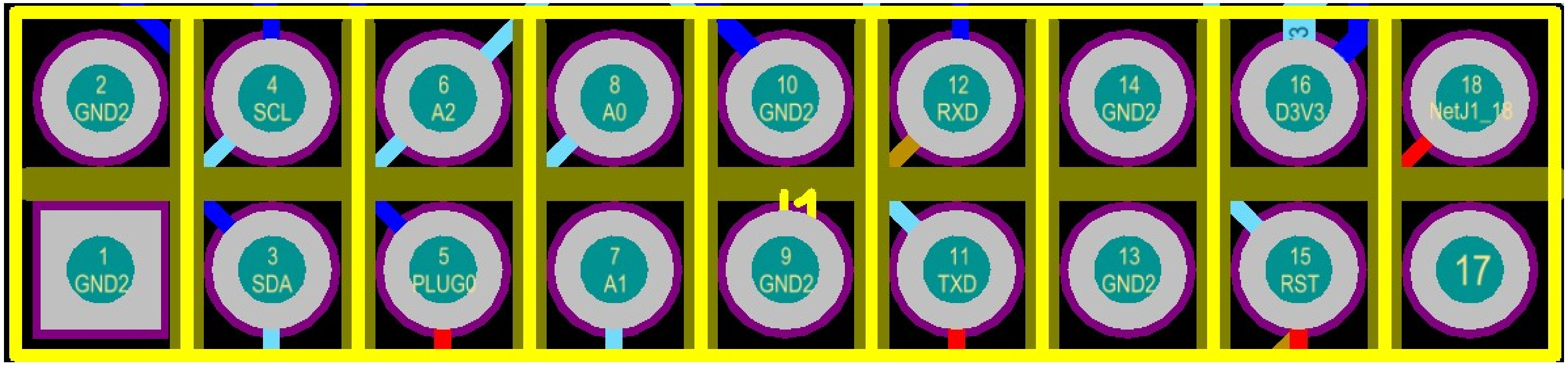

2 GND2
4 SCL
6 A2
8 A0
10 GND2
12 RXD
14 GND2
16 D3V3
18 NetJ1_18
1 GND2
3 SDA
5 PLUG0
7 A1
9 GND2
11 TXD
13 GND2
15 RST
17
J1

Fig 8. Each Pin Definition of IO

As shown in above fig:

Pin 1, 2, 9, 10, 13, and 14: GND.

Pin 3 and 4 (SDA, SCL): the I²C bus wire of DC-DC PIC, connect control panel to communicate with PIC; through which control panel can read and write PIC data, and thereby control the running state of hashboard.

Pin 5 (PLUG0): identification signal of hashboard, this signal raises 10K resistance to 3.3V by hashboard, so this pin is high level (because 3.3V voltage is powered by pin 16 of control panel) when IO signal is plugged.

Pin 6, 7 and 8 (A2, A1, A0): PIC address signal.

Pin 11 and 12 (TXD, RXD): hash rate channel of hashboard, and changes into TX (CO), RX (RI) signals through resistive voltage division; the electrical level of all IO mouth pin ends is 3.3V, and changes into 1.8V through resistive voltage division.

Pin 15 (RST): reset signal 3.3V end, and changes into 1.8V RST reset signal through resistive voltage division.

Pin 16 (D3V3): hashboard 3.3V power supply, this 3.3V is powered by control panel, and mainly supplies working voltage to PIC.

Below Fig 9 and Fig 10 show the voltage and distribution of each pin of IO before and after voltage division.

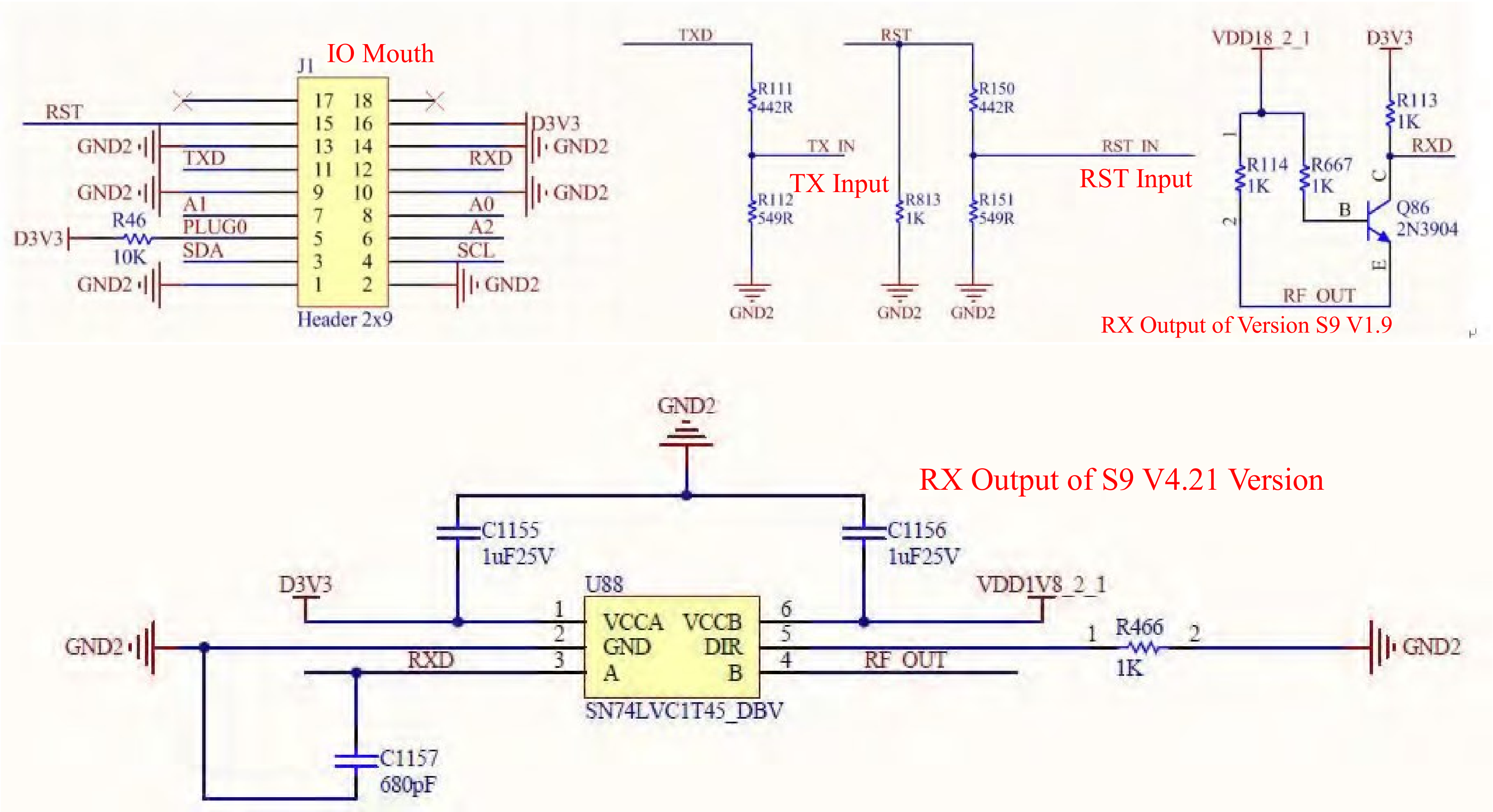

IO Mouth
J1
RST
GND2
TXD
GND2
A1
R46
D3V3
PLUG0
10K
SDA
GND2
17 18
15 16
13 14
11 12
9 10
7 8
5 6
3 4
1 2
Header 2x9
D3V3
GND2
RXD
GND2
A0
A2
SCL
GND2
TXD
R111
442R
TX_IN
TX Input
R112
549R
GND2
RST
R813
1K
GND2
R150
442R
RST_IN
RST Input
R151
549R
GND2
VDD18_2_1
D3V3
R113
1K
RXD
R114
1K
R667
1K
B
C
E
Q86
2N3904
RF_OUT
RX Output of Version S9 V1.9
GND2
RX Output of S9 V4.21 Version
C1155
1uF25V
C1156
1uF25V
D3V3
U88
VDD1V8_2_1
GND2
RXD
VCCA
GND
A
VCCB
DIR
B
1
2
3
6
5
4
RF_OUT
R466
1K
GND2
SN74LVC1T45_DBV
C1157
680pF

Fig 9. Each Division Voltage of IO Signal of S9

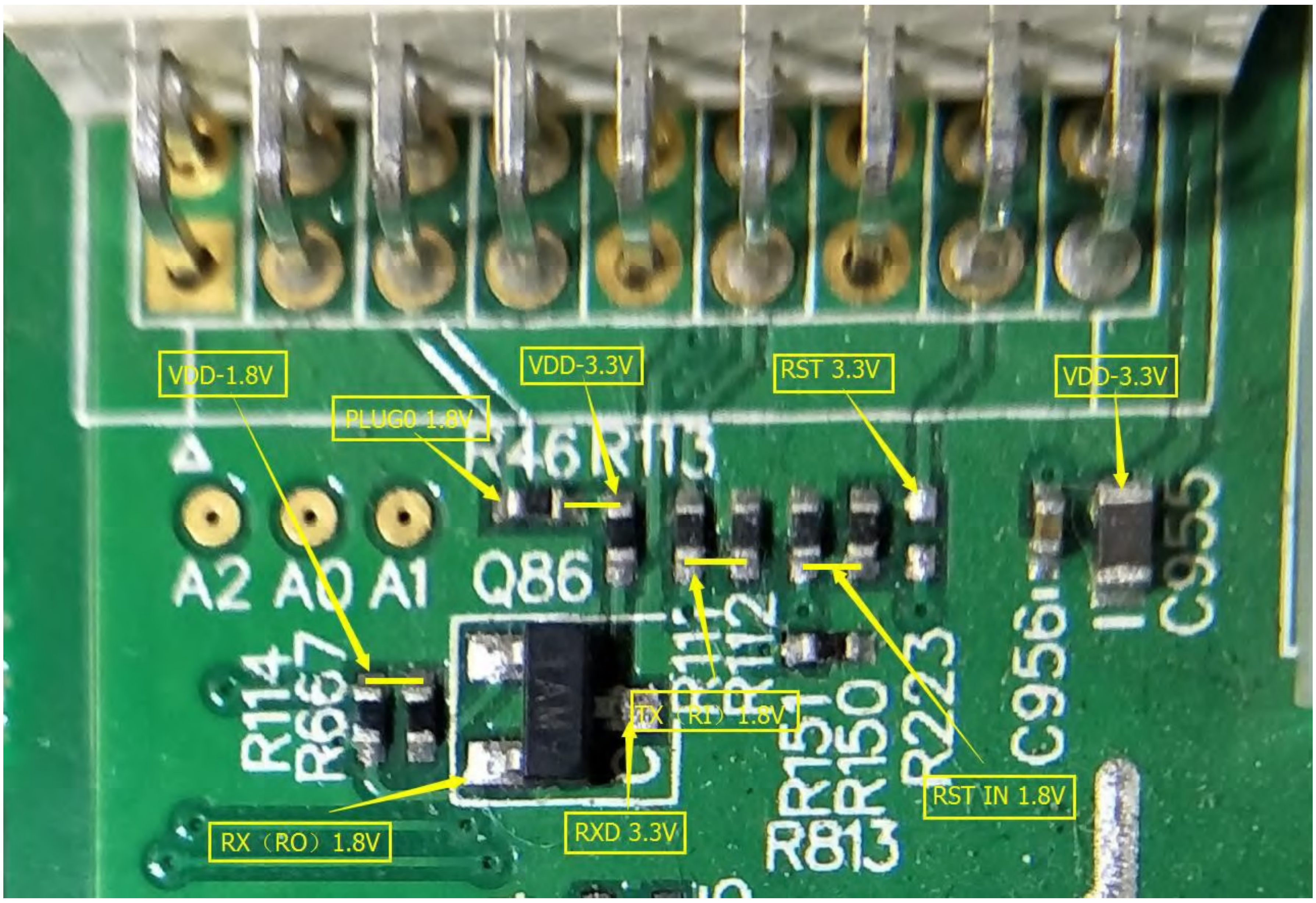

VDD-1.8V
PLUG0 1.8V
VDD-3.3V
RST 3.3V
VDD-3.3V
R46 R113
A2 A0 A1
Q86
R114
R667
R111
R112
TX（RI）1.8V
R151
R150
R223
C956
C955
RST IN 1.8V
RXD 3.3V
RX（RO）1.8V
R813

Fig 10. Each Division Voltage of IO Signal in 1.9 Version

4. The Power Supply Circuits of the Last 5 Voltage Domains

❶ 14V Booster Circuit:

The responsibility is to boost DC-DC (8.3 - 9.2V) to 14V, and the principle is to boost 9V to 14V through U110 RT8537 switching power supply, the switching signal produced by U110 becomes inductive energy storage via L1, and then becomes boost rectifying diode via D100 to charge and discharge C954, and thereby get the 14V of C954 positive electrode. See Fig 11 and Fig 12:

❷ the power supply of the last five voltage domains without 14V boosted circuits are from 12V input power source.

The power supply of the last five voltage domains without 14V boosted circuits are from 12V input power source.

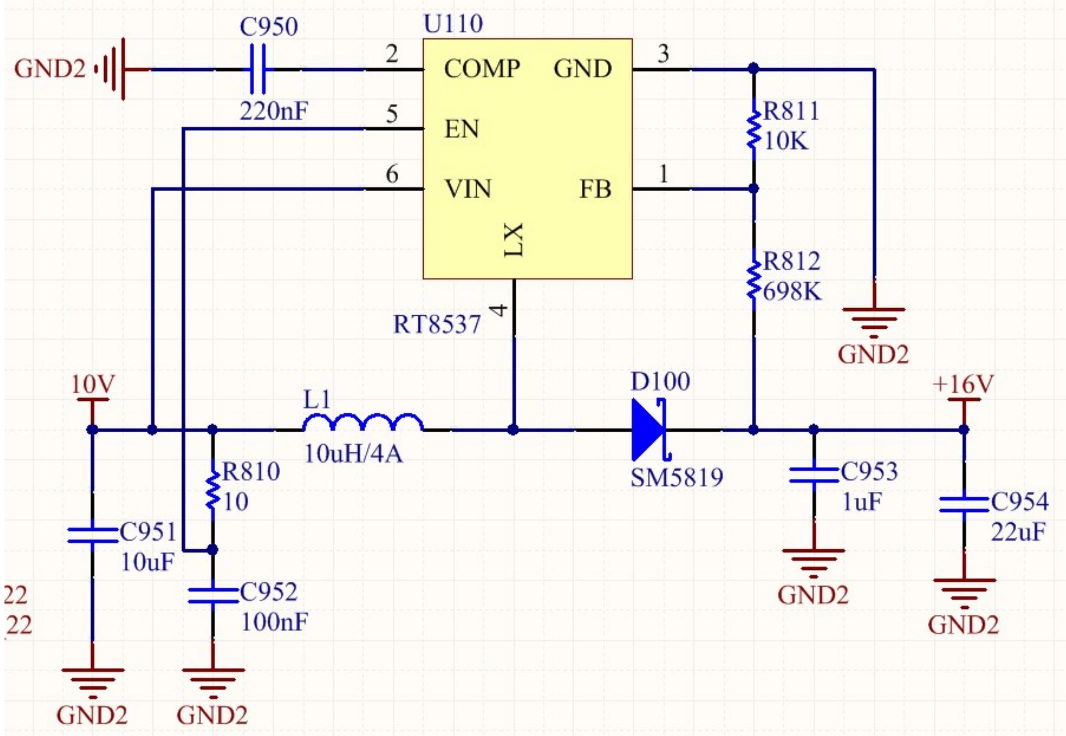

GND2
C950
220nF
U110
2
COMP
GND
3
5
EN
R811
10K
6
VIN
FB
1
LX
R812
698K
RT8537
4
GND2
10V
L1
10uH/4A
D100
SM5819
+16V
R810
10
C953
1uF
C954
22uF
C951
10uF
C952
100nF
22
22
GND2
GND2
GND2
GND2

Fig 11. 14V Boost Schematic Diagram

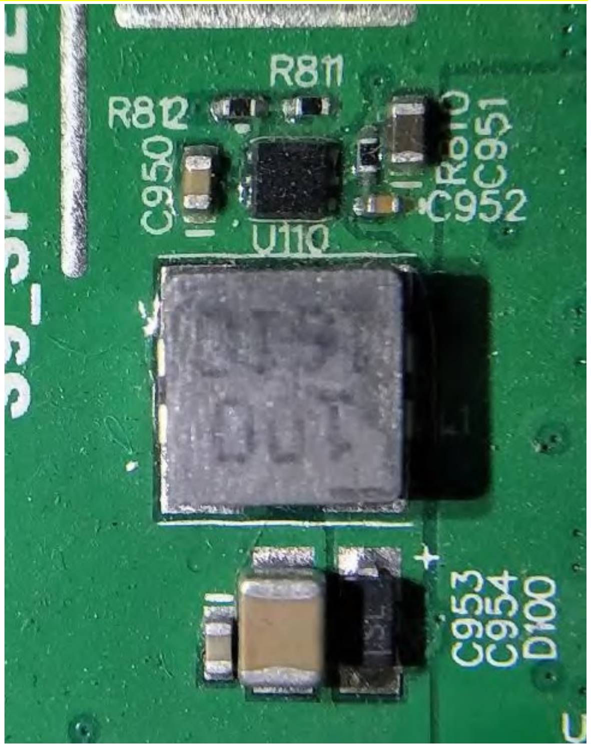
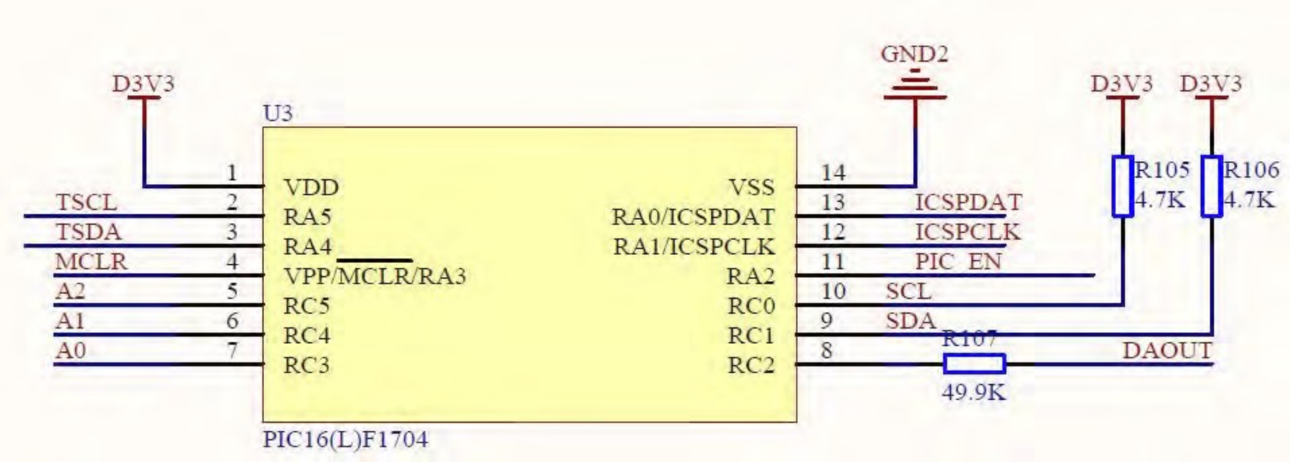

R811
R812
C950
U110
R810
C951
C952
C953
C954
D100

Fig 12. 14V Boost PCB

Note: the voltage anomaly of booster circuit often causes the LDO damage of the last 5 voltage domains of hashboard, and also causes chip damage easily. And the anomaly of boost voltage is often caused by the oxidation of U110, R812 and R811.

5. DC-PIC: Composed of PIC16(L)F1704. See Fig 13 and Fig 14:

The device stores the frequency information and voltage value of the chip of hashboard, through which we can control the DC-DC output voltage of hashboard.


D3V3
U3
GND2
D3V3
D3V3
1 VDD
2 RA5
3 RA4
4 VPP/MCLR/RA3
5 RC5
6 RC4
7 RC3
14 VSS
13 RA0/ICSPDAT
12 RA1/ICSPCLK
11 RA2
10 RC0
9 RC1
8 RC2
TSCL
TSDA
MCLR
A2
A1
A0
ICSPDAT
ICSPCLK
PIC_EN
SCL
SDA
R105 4.7K
R106 4.7K
R107 49.9K
DAOUT
PIC16(L)F1704

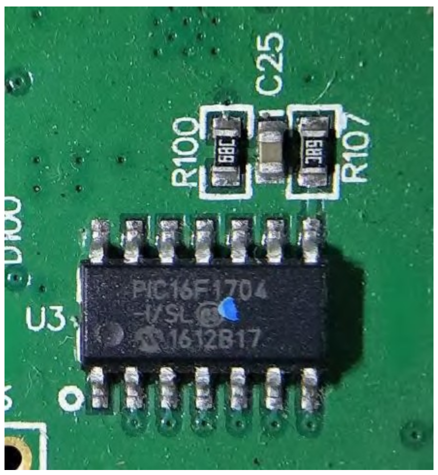

C25
R100
R107
U3
PIC16F1704
-I/SL
1612B17

Fig 13. PIC Schematic Diagram

Fig 14. PIC Circuit

When PIC works, it needs to control and send a heartbeat signal every minute. Without heartbeat information, PIC will be closed after one minute. PIC pin 1 is VDD 3.3V, pin 14 is GND, pin 9 and 10 are I²C bus wire that connects IO mouth to control panel, pin 5, 6 and 7 are PIC addresses; pin 4 is PIC 3.3V; pin 8 is the FB output of PIC, and controls DC-DC voltage; pin 11 is EN signal that PIC outputs, and controls DC-DC operational status.

6. DC-DC Circuit: Composed of LM27402SQ and CMOS tube TPHR9003NL. See below Fig 15 and Fig 16:

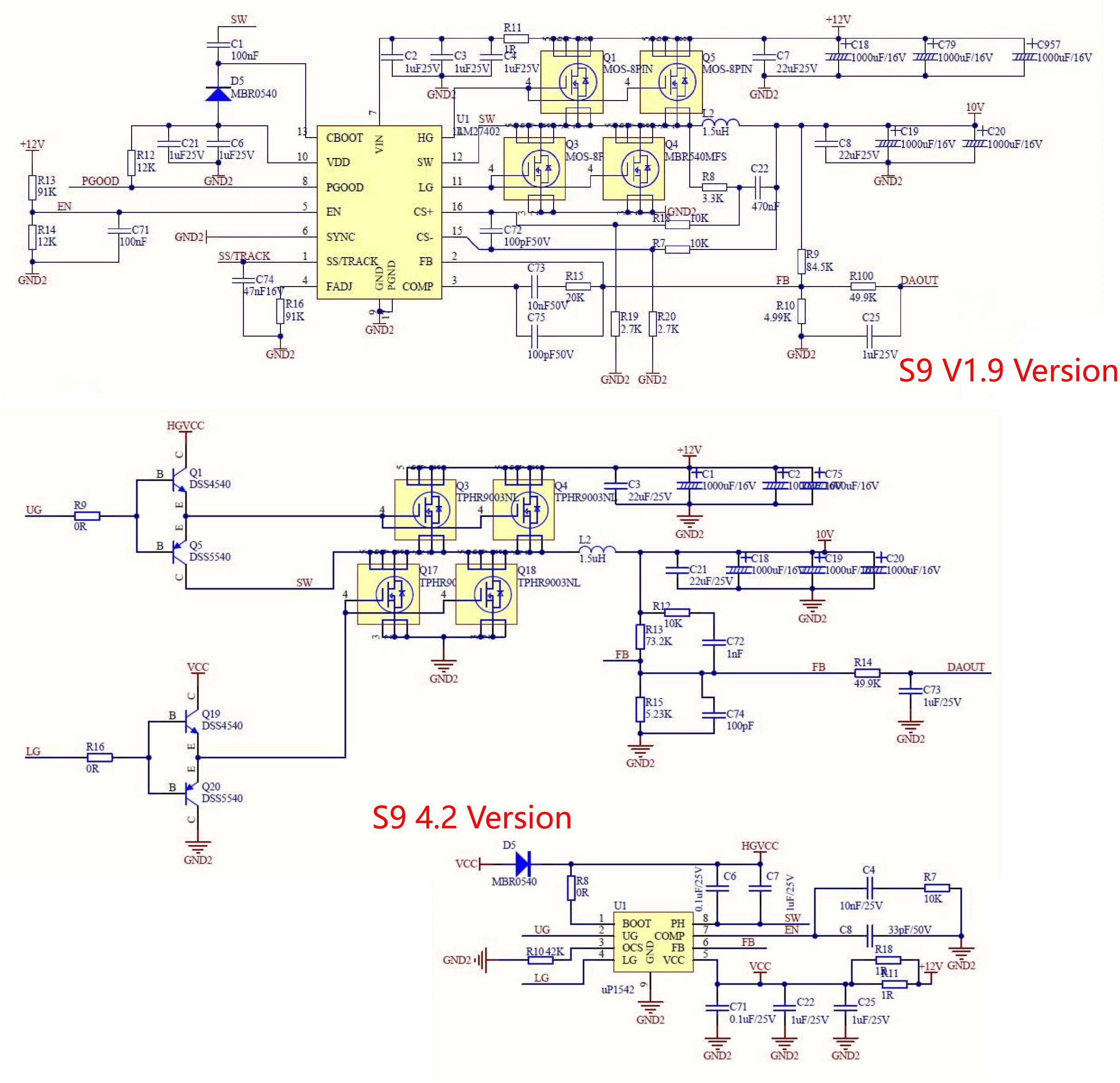

SW
C1 100nF
D5 MBR0540
+12V
R12 12K
C21 1uF25V
C6 1uF25V
R13 91K
PGOOD
EN
R14 12K
C71 100nF
GND2
SS/TRACK
C74 47nF16V
R16 91K
CBOOT
VDD
PGOOD
EN
SYNC
SS/TRACK
FADJ
VIN
HG
SW
LG
CS+
CS-
FB
COMP
GND
PGND
U1 LM27402
C2 1uF25V
C3 1uF25V
C4 1uF25V
R11 1R
Q1 MOS-8PIN
Q5 MOS-8PIN
Q3 MOS-8P
Q4 MBR540MFS
C7 22uF25V
C18 1000uF/16V
C79 1000uF/16V
C957 1000uF/16V
L2 1.5uH
10V
C8 22uF25V
C19 1000uF/16V
C20 1000uF/16V
R8 3.3K
C22 470nF
R18 10K
R7 10K
C72 100pF50V
C73 10nF50V
R15 20K
C75 100pF50V
R19 2.7K
R20 2.7K
R9 84.5K
R100 49.9K
DAOUT
R10 4.99K
C25 1uF25V
S9 V1.9 Version
HGVCC
UG
R9 0R
Q1 DSS4540
Q5 DSS5540
Q3 TPHR9003NL
Q4 TPHR9003NL
C3 22uF/25V
+12V
C1 1000uF/16V
C2
C75 1000uF/16V
L2 1.5uH
Q17 TPHR9003NL
Q18 TPHR9003NL
C21 22uF/25V
C18 1000uF/16V
C19 1000uF/16V
C20 1000uF/16V
R12 10K
R13 73.2K
C72 1nF
FB
R14 49.9K
DAOUT
C73 1uF/25V
R15 5.23K
C74 100pF
VCC
LG
R16 0R
Q19 DSS4540
Q20 DSS5540
S9 4.2 Version
D5 MBR0540
R8 0R
U1
BOOT
UG
OCS
LG
PH
COMP
FB
VCC
uP1542
C6 0.1uF/25V
C7 1uF/25V
C4 10nF/25V
R7 10K
C8 33pF/50V
EN
R10 42K
R18 1R
R11 1R
C71 0.1uF/25V
C22 1uF/25V
C25 1uF/25V
GND2

Fig 15. DC-DC Schematic Diagram

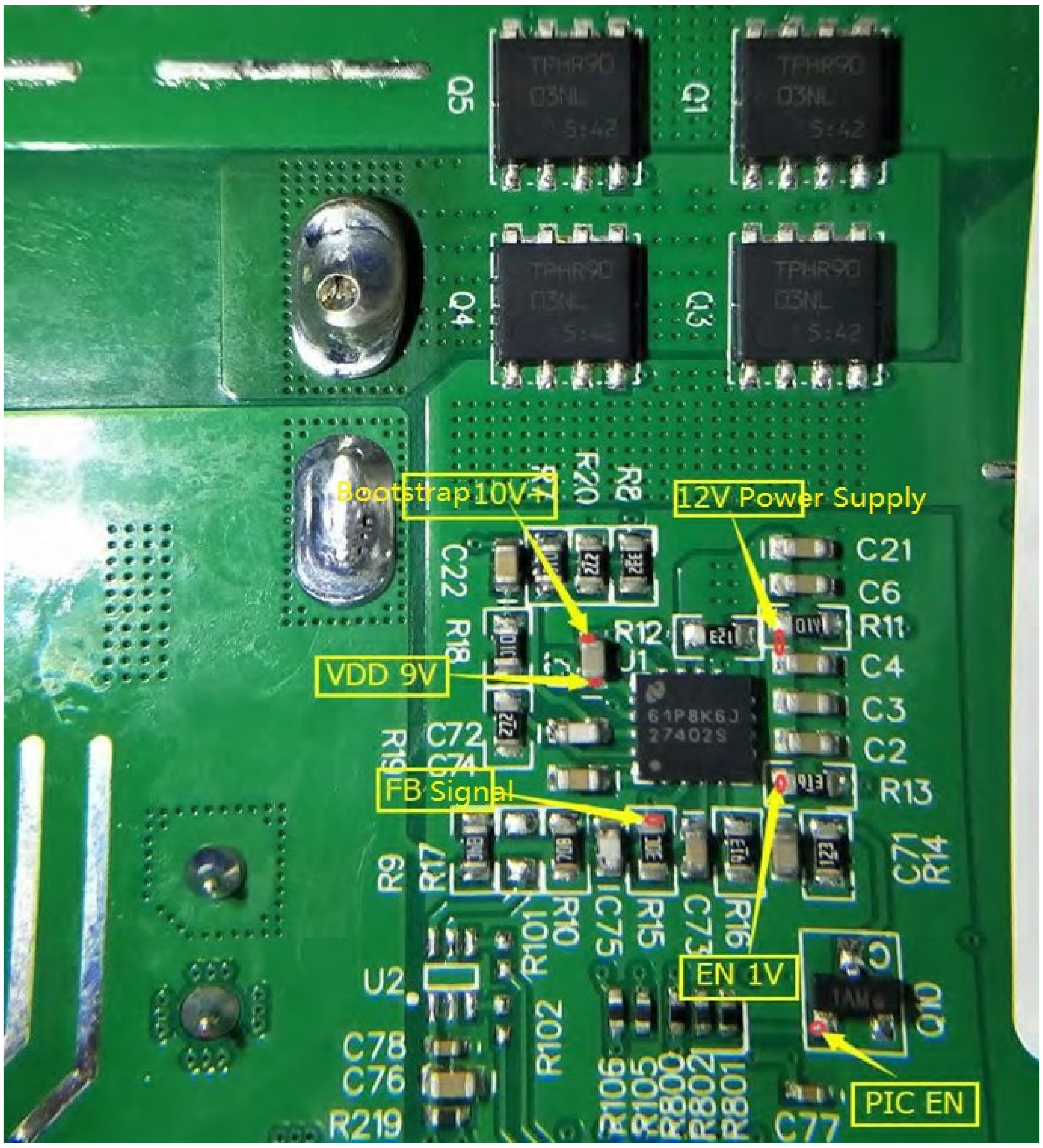

Q5
Q1
Q4
Q3
TPHR90 03NL
Bootstrap 10V+
R20
R8
12V Power Supply
C21
C6
R11
C4
C3
C2
R13
C22
R18
R12
J1
VDD 9V
C72
C74
R19
FB Signal
R9
R17
R101
R10
C75
R15
C73
R16
C71
R14
EN 1V
U2
C78
C76
R219
R102
R106
R105
R800
R802
R801
C77
PIC EN
Q10

Fig 16. DC-DC Circuit

This figure takes version S9 V1.9 for example

LM27402SQ voltage regulator produces PWM switching signal to drive upper and lower bridges (two pairs of CMOS), and stores energy via L2 inductance, and then filters via C19 and C20.

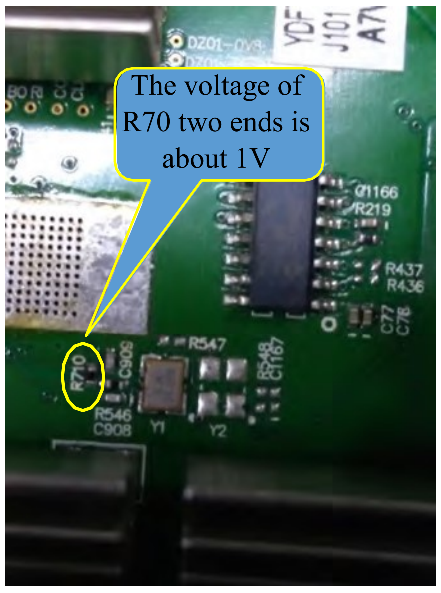
LM27402SQ main function pins:
Pin 7: 12V power supply,
Pin 9 and 17: GND
Pin 2: FB feedback, connect PIC, and the voltage is decided by Pin 8 of PIC.
Pin 10: VDD
Pin 13: bootstrap capacitor 10V+
Pin 16: impulse
Pin 12: switching signal
Pin 11: lower bridge drive
Pin 14: upper bridge drive

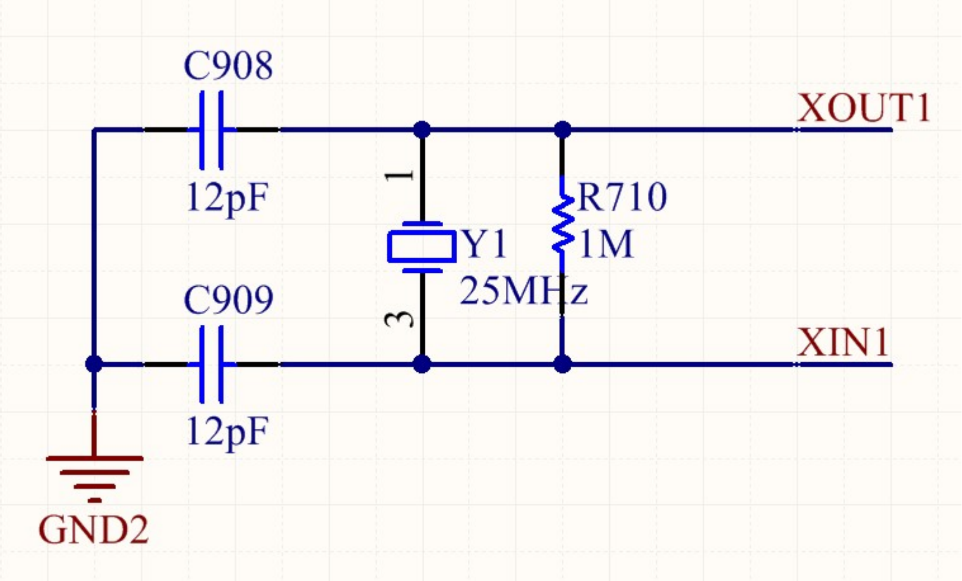
When the voltage of DC-DC is abnormal, firstly check the consistency of PIC voltage value and DC-DC output voltage via tool print information; if they are inconsistent, replace the low capacitance around LM27402SQ;

If DC-DC has no output, check whether the EN voltage of R13 and R14 is about 1V, R11 voltage is 12V, PIC is in normal operation, and whether PIC can receive I^{2}C signal of control panel normally.

The standard of DC-DC output voltage:
14T hashboard: 8.3V-8.6V
13.5T hashboard: 8.4V-8.7V
13T hashboard: 8.4V-8.9V
12.5T hashboard: 8.5V-9.1V
Under 12T hashboard: 8.6-9.2V
Out of these scopes, check DC-DC circuit.

7. 25M CLK: Composed of Y 25MHZ passive crystal oscillator and 12pF: See Fig 17 and Fig 18. d


The voltage of R70 two ends is about 1V
R710
C908
R546
R547
Y1
Y2
R437
R436
R219


C908
12pF
XOUT1
1
R710
1M
Y1
25MHz
3
C909
12pF
XIN1
GND2

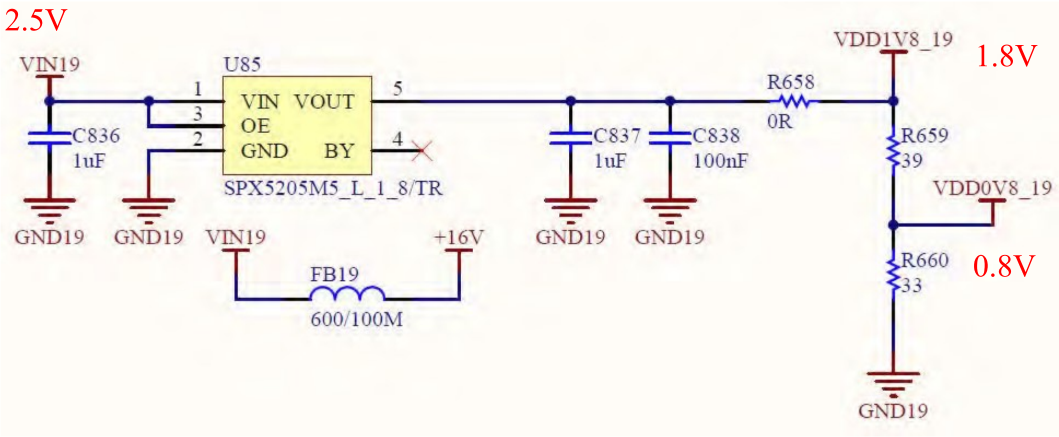
Normally, the voltage of R70 two ends is about 1V

Fig 17. 25M CLK Circuit

Fig 18. 25M CLK Schematic

8. 1.8V-LDO: Composed of 1.8VLDO SPX5205M5_L_1_8.

See below Fig 19 and Fig 20:
SPX5205M5, Pin 1 and 3 in, Pin 5 1.8V out;
Note: the LDO power supply of S9 hashboard has two types. The first type is that every voltage domain of hashboard has an external LDO SPX5205M5, responsible for the LOD of the 3 chips of each voltage domain; the other type is that only the last 5 voltage domains have external LDO, and other voltages are powered by chip built-in LDO; all BM1387 chips have built-in LDO power supply circuit, BM1387 pin 14 (LDO-25I) in, pin 12(LDO-18O) out, and each chip has independent LDO without mutual interference. The LDO-25I power supply of the last 5 voltage domains with 14V booster circuit are from 14V booster circuit, and the power supply of the last five voltage domain without 14V booster circuit are from 12V input power source; and the LDO-25I of other voltage domains are from chip itself.
PLL-08 voltage is from LOD-1.8 via voltage division of two resistances.


2.5V
VIN19
U85
1
3
2
VIN VOUT
OE
GND BY
5
4
SPX5205M5_L_1_8/TR
C836
1uF
GND19
GND19
VIN19
+16V
FB19
600/100M
C837
1uF
C838
100nF
GND19
GND19
VDD1V8_19
1.8V
R658
0R
R659
39
VDD0V8_19
R660
33
0.8V
GND19

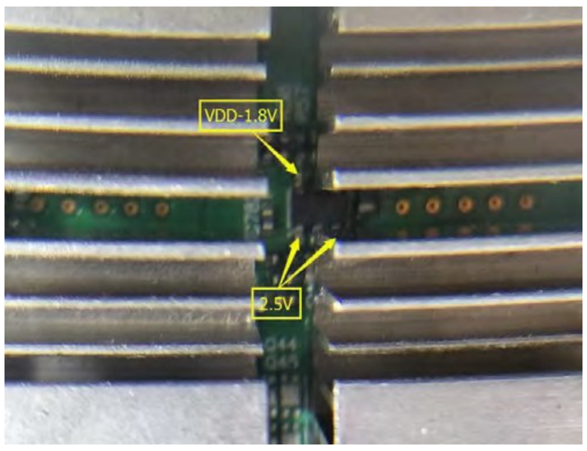
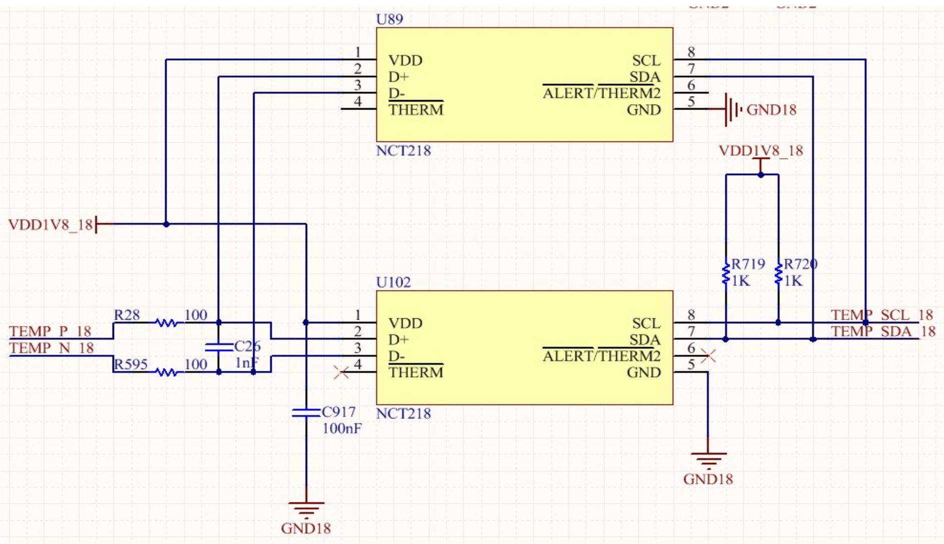


Fig 19. 1.8V Voltage Stabilizing Circuit

Fig 20. 1.8V Voltage Stabilizing Circuit

9. Temperature sensor circuit: two temperature sensors, one is TEMP (PCB), consisting of sensor IC; the other is TEMP (CHIP), composing of chip build-in temperature sensor group (BM1387 pin 15 and pin 16). The two temperature sensors collect parameter, and return to FPGA of control panel from RI via BM1387 pin 17 and pin 18. The principle is as Fig 21: The normal temperature range of the chip of S9 Miner Temp (Chip2) is 65-125 degrees Celsius, and the max running temperature of miner chip is degrees Celsius. When exceeding the range, red light blinks and gives an alarm, and machine halts for protection.


U89
1
2
3
4
VDD
D+
D-
THERM
SCL
SDA
ALERT/THERM2
GND
8
7
6
5
GND18
NCT218
VDD1V8_18
VDD1V8_18
R719
1K
R720
1K
U102
TEMP_P_18
TEMP_N_18
R28
100
R595
100
C26
1nF
VDD
D+
D-
THERM
SCL
SDA
ALERT/THERM2
GND
TEMP_SCL_18
TEMP_SDA_18
C917
100nF
NCT218
GND18
GND18

The chips that S9 V1.9 version temperature sensor I^{2}C bus wire (TEMP_SDA, TEMP_SCL) connect are: No. 62(U66), 46(U50), 25(U29) and 2(U10) chips

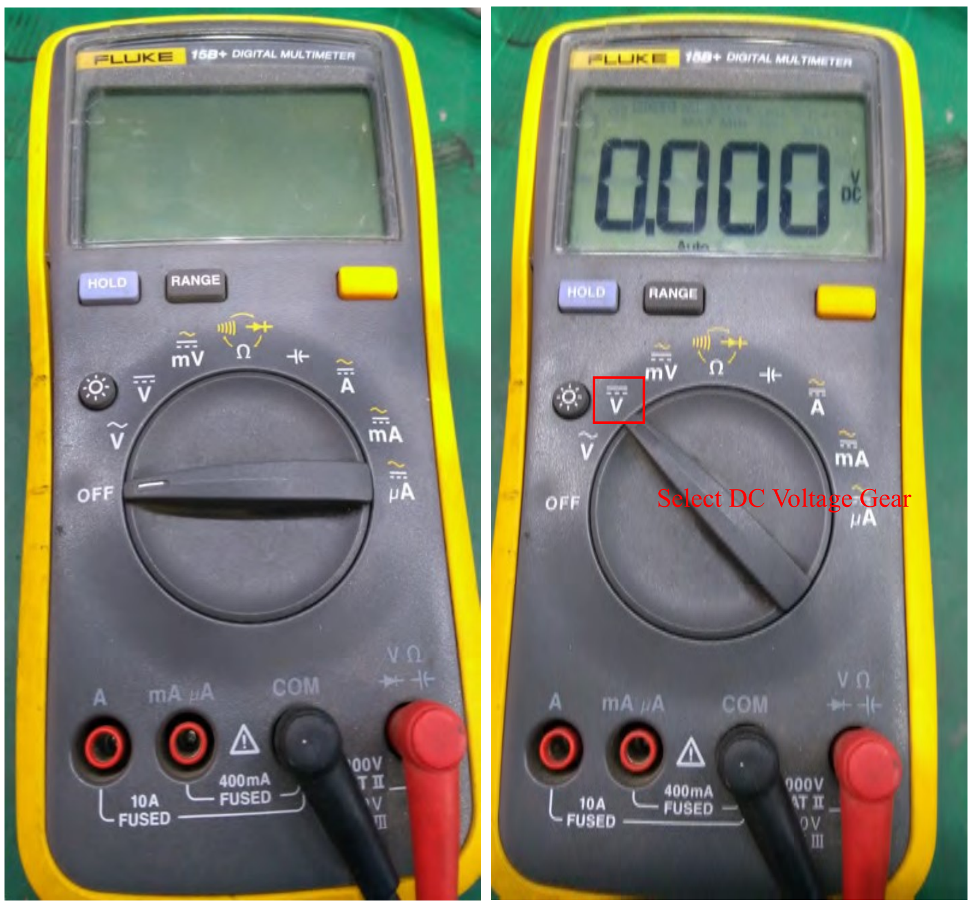
Fig 21. Temperature Sensor Schematic Diagram

IV. Preparation before Maintenance

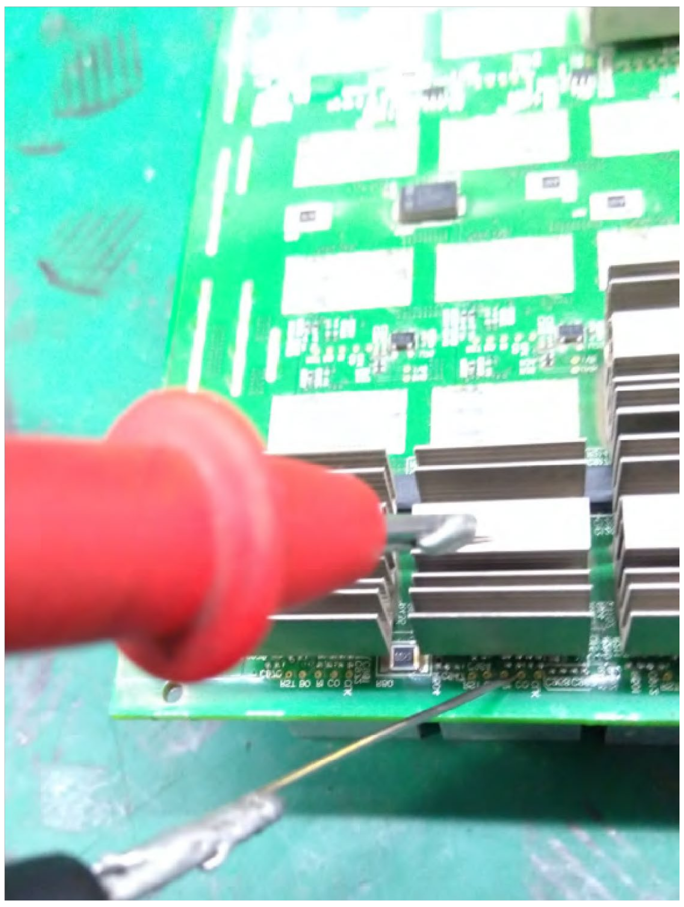
1. The Application Method of Multimeter:

※Unless otherwise stated, the tested results of voltages and resistances involved in this document are all subject to the results tested by the multimeter of FLUKE 15B+ model (great error exists among different brands and models)

① The Gear Selection and Measuring Method of Voltage Measurement



❶ Gear Selection

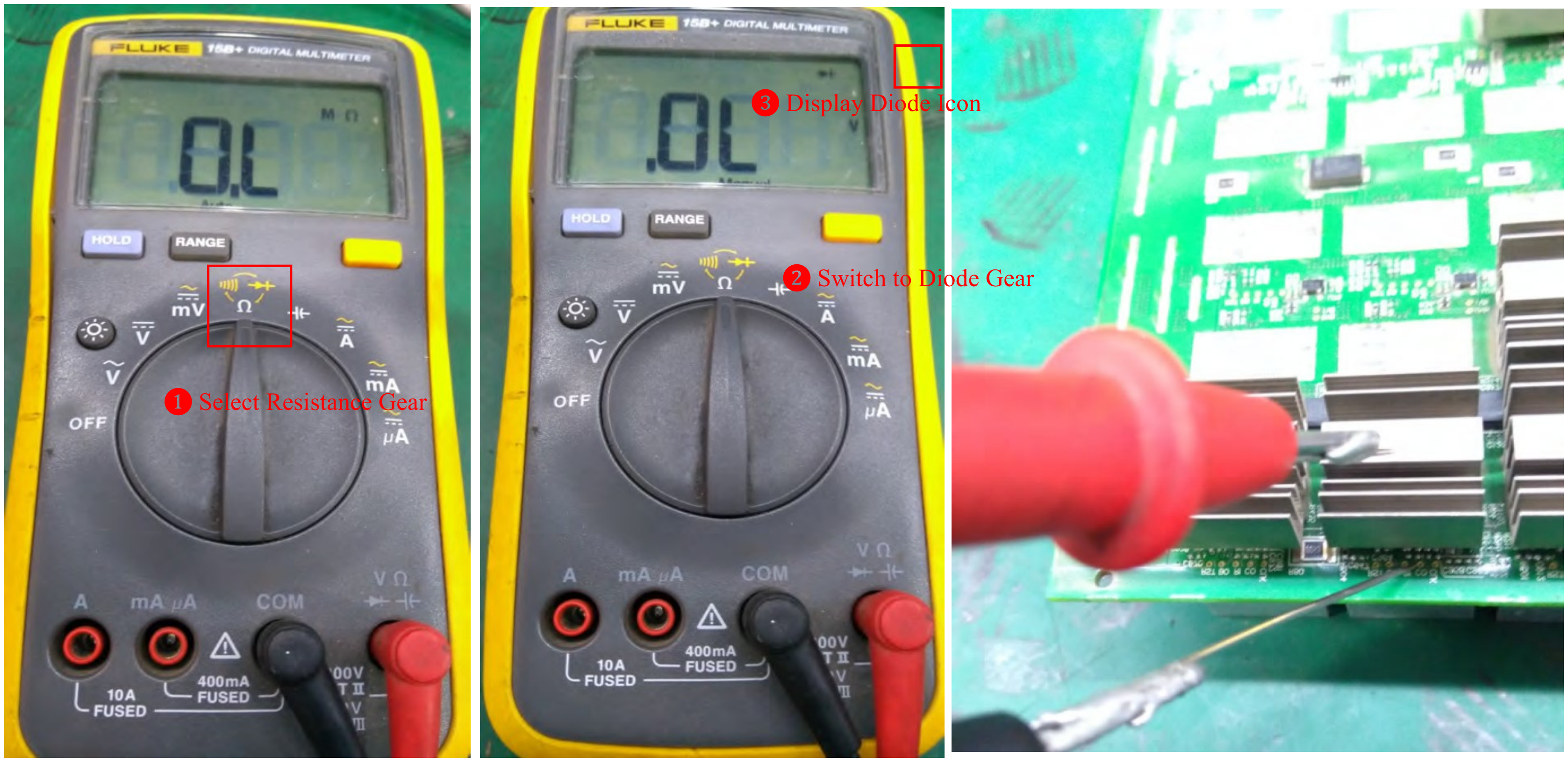


❷ Measuring Voltage

I. This machine is powered by external power supply, so this machine only has DC power supply, and thereby select DC voltage gear of multimeter.

II. Red probe grounding and black probe grounding need no distinction for digital multimeter. When the probes are connected reverse, "-" appears. However, note that hashboard has 21 voltage domains in total, and each voltage difference between the domains is 0.4V. Therefore, probe should connect the ground of the voltage needing to measure.

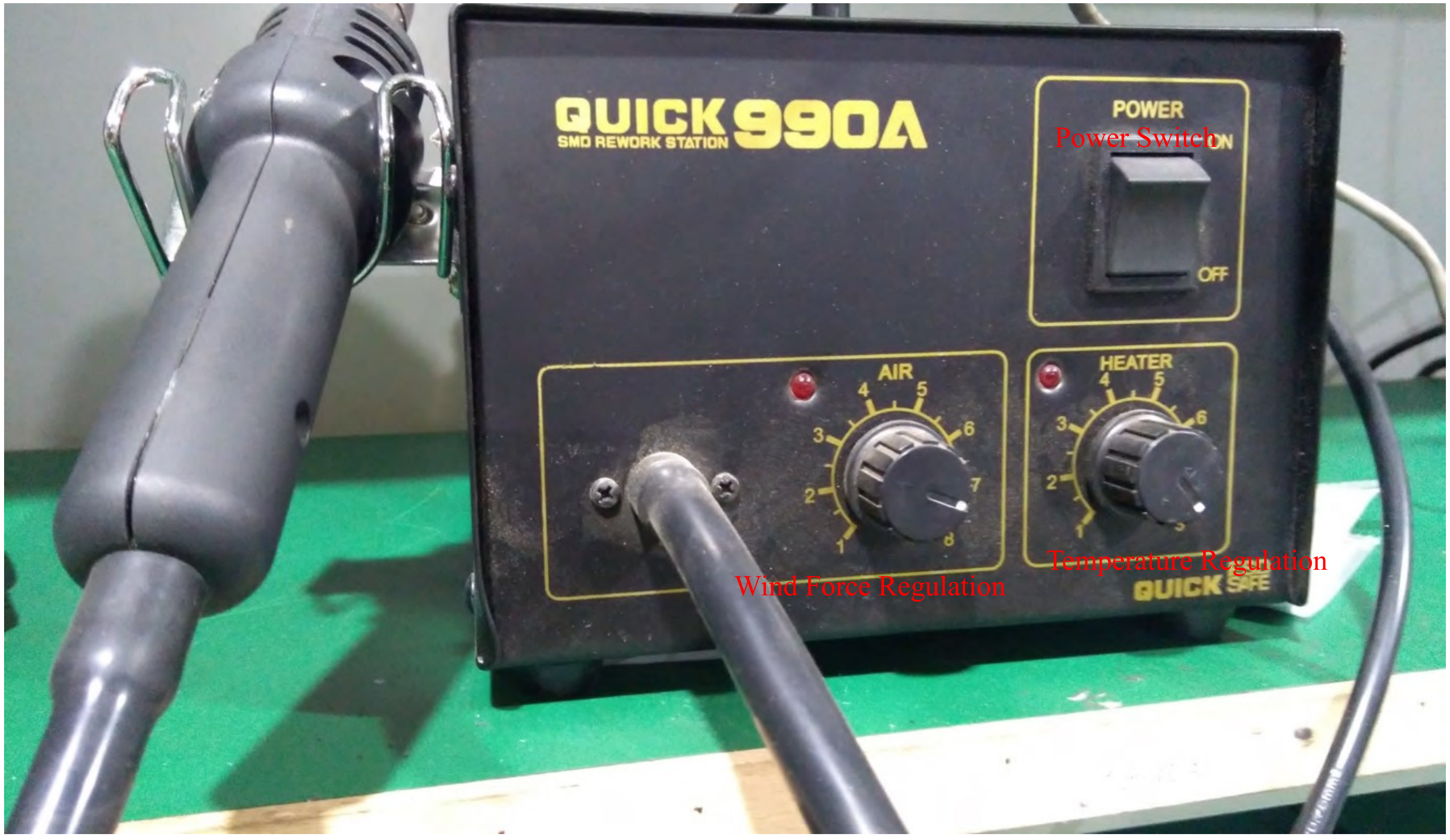
② The Measuring Method of Resistance



1. Firstly, switch the multimeter to resistance gear, and then press yellow button to shift gear, until the screen displays the diode icon, which means multimeter has tuned to diode gear.
2. Measure resistance. The resistances measured via diode involved in this course all refer to reverse resistance, that is, the resistance tested by black probe when red probe is grounded. In other words, keep red probe grounding, black probe measures the place in need of measurement.

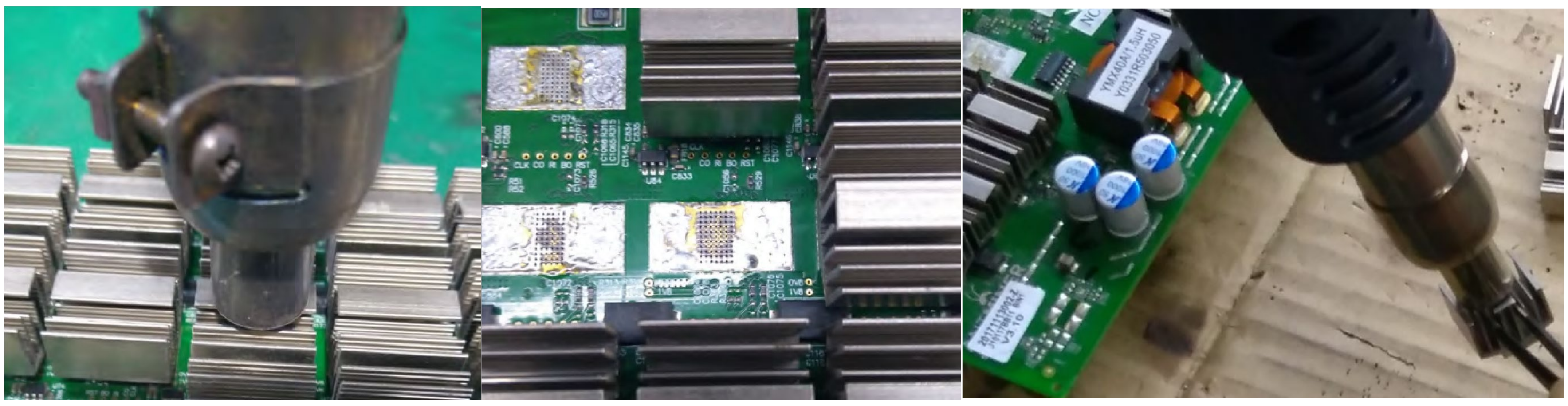
2. The Application Method of Heat Gun and the Assembly and Disassembly Techniques of Chip

※QUICK990AD soldering station with temperature display is recommended



I. The Application Method of Heat Gun: firstly, switch on and adjust to proper temperature, heat gun with temperature display is recommended to buy, about 360℃ in general, depending on the specific environmental temperature, and then adjust to proper wind force.
Switch off the power when not in use for a long time. This product will produce high temperature, beware burn! When switching off, heat gun will not immediately power off before temperature drops to a certain degree, please be patient.

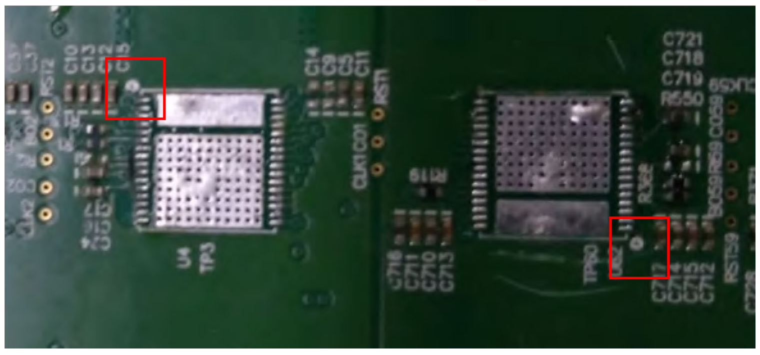
II. The Assembly and Disassembly Techniques of Chip



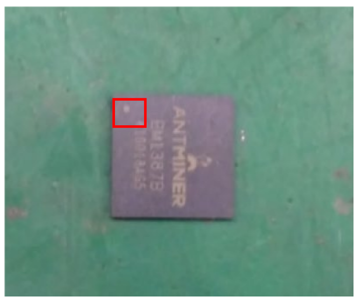
Disassemble the cooling fin on the back, heat the cooling fin on the back until the temperature is high enough to melt tin, and then use tweezers to remove it. In assembly, heat outside first until the temperature is high enough to melt tin, place the cooling fin on the pad and press.

With regard to the cooling fin on the front, blow while tilt the cooling fin. After the cooling fin is removed, take advantage of heat and use scraper to clean the heat-conducting glue (black) on the side adhere to chip thoroughly. Then slightly heat the surface of chip and use scraper to clean up the black glue on it. Put aside the chip when quality is unknown, and the poor ones should be classified according to fault classification.
In the assemble of cooling fin on the front side, put black glue on chip, outside heat cooling fin until the temperature is high enough, and then quickly put the cooling fin on chip and press after adjusting the direction properly, wait the solidification of the black glue.

3. The Identification of Chip Direction

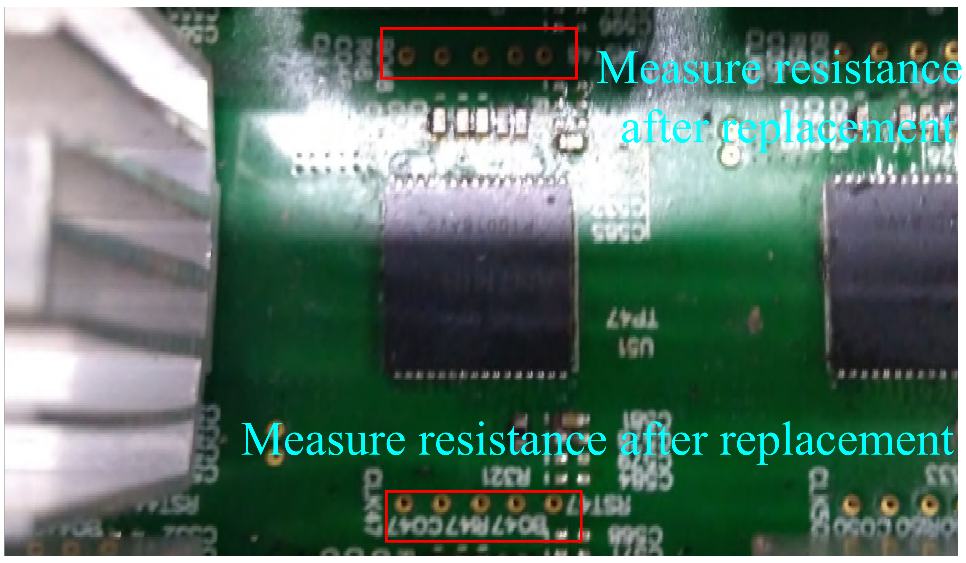


It is Pin 1 of the chip where there is round spot on pad



It is Pin 1 of the chip where there is round spot

The above identification method is applicable to all chips


Measure resistance after replacement
Measure resistance after replacement

4. Replace a chip and let it cool, then measure the 10 test points on the two sides of the chip, to see whether their resistances are normal. Have power-on test when all resistances are normal. Otherwise, reweld the chip until resistances under measurement are normal.

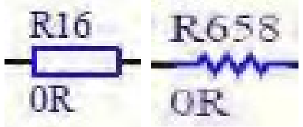
When resistances are abnormal, power on is very likely to burn the chip due to pin is not justified, solder bridge, false welding, etc., and cause the damage of new chip before starting work

5. The Basic Knowledge of Electronic Components

Electronic component: refers to the finished product whose molecular components have not been changed during production and processing in factory, such as resistor, capacitor and inductance. Because it does not produce electron itself and has no effect on voltage and current, it is also called passive device.
Electronic device: refers to the finished product whose molecular structure has been changed during the production and processing in factory, such as transistor, electron tube and integrated circuit. Because it can produce electron itself and has effect on voltage and current (amplification, on-off, rectification, detection, oscillation, modulation, etc.), it also called active device.

① Resistance (R): the inhibition of conductor to current is usually known as resistance. Letter R is always used to represent resistance. The unit of Resistance is ohm, and the symbol is Ω. Kioohm (kΩ) and megaohm (MΩ) are also units commonly used.

The symbol of resistance in circuit



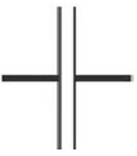
Color Ring (DIP) Resistor

Chip Resistor

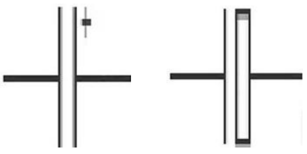
The numerical reading of color ring resistor: in 4-color ring resistor, the first and second are numerical number, the third is the multiple of 10^n, the forth is error; 5-color ring resistor: from the first to the third are numerical number, the fourth is the multiple of10^n, and the fifth is error
The numerical numbers that the colors of color ring resistor represent: brown 1, red 2, orange 3, yellow 4, green 5, blue 6, purple 7, grey 8, white 9, black 0, golden 10^{-1}, silvery 10^{-2}, error: golden ±5%, silvery ±10%, achromatic ±20%, brown ±1%
According to above method, the computing method of the color ring resistor of above Fig can be known: brown=1 black=0 brown=1 golden=±5%, resistance of this resistor is: 1 (the first reading number) 0 (the second reading number) $\times 10^1$ (the third reading number) ±5% (the fourth reading number) = 100Ω±5%
The golden and silvery that are in the third place of 4-color ring resistor and the fourth place of 5-color ring resistor, represent their multiple; are in the last ring, represent their error
The resistance of chip resistor can be computed according to above numerical number

② Capacitance (C): Capacitor is a kind of energy storing element, composing of two conductors which are insulated and close to each other, and a layer of non-conducting insulating media. The two conductors become the two poles of capacitor and are drew forth by conducting wire respectively. They are used for tuning, oscillation, separation, wave filtering, interconnection, bypass, etc. Capacitance is one of the most commonly used and most basic electronic components.
Capacitance use C to represent, its unit is F(farad), and common units include µF(microfarad), pF(picofarad), etc. Conversion of units: 1F=10^6uF=10^{12}pF

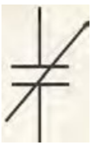
The symbols of capacitance in circuit Non-polar Capacitor



Electrolytic Capacitor



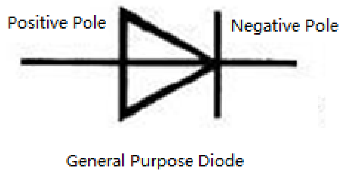
Variable Capacitor



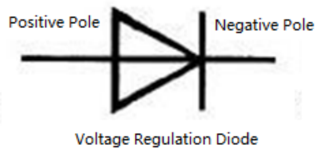
The capacity of capacitance: for DIP Capacitor, the capacity is always marked on the surface in numerical form; for Multiplayer Ceramic Chip Capacitors, the capacity is marked on material plate and the material itself has no mark. Please require BOM table or circuit schematic diagram if needed.

③ Diode (D): Characteristics: unilateral conductivity (current can only flow from positive pole to negative pole)
Functions: rectification, on-off (general purpose diode), etc.

The symbols of diode in circuit General Purpose Diode



Voltage Regulation Diode



Light Emitting Diode

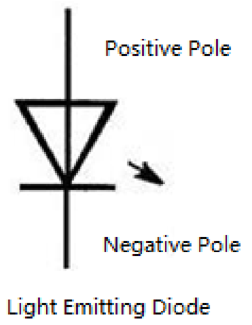
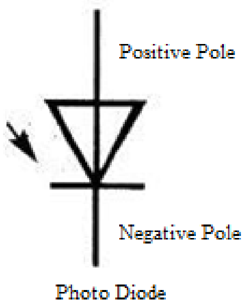
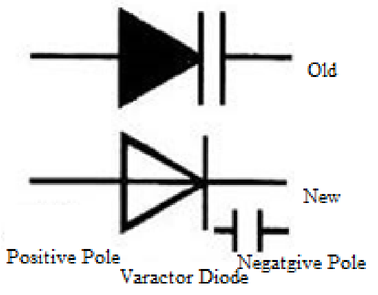


Photo Diode

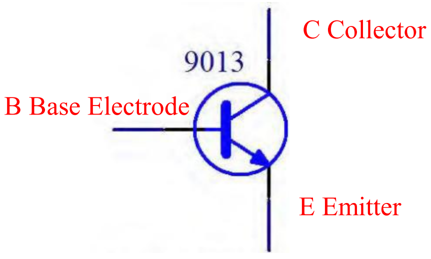


Varactor Diode



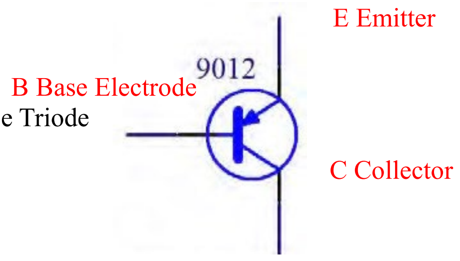
④ Triode (Q): The functions of triode: on-off, amplification Two Main Types of Triode: NPN and PNP

The symbols of triode in circuit NPN Type Triode



NPN Type Triode

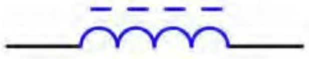
PNP Type Triode



PNP Type Triode

❺ Inductance (L): magnetic induction is formed when current passes through coil, and then magnetic induction produces induced current to resist the current that passes through coil. We call this kind of interaction between current and coil inductive reactance of electricity, that is, inductance. The unit is “Henry” (H). This property also can be used to make inductors. Inductor is generally composed of framework, winding, screening can, packaging material (packaging material adopts plastic, epoxide resin, etc.), magnetic core, iron core, etc.

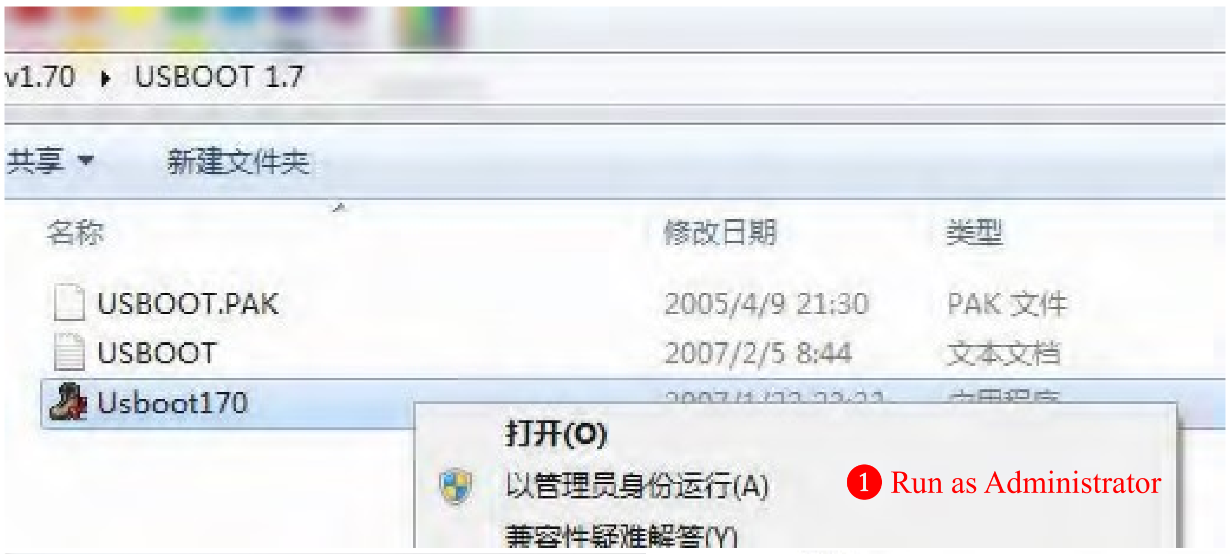
The symbol of inductance in circuit



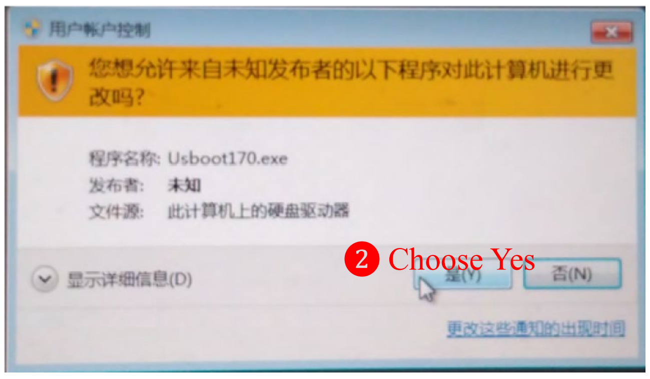
The functions of inductance: oscillation, wave filtering

6. Hashboard Tester T Card Making

I. T Card Capacity Recovery: This step is only for the T card that has already used or is in need of reburning in model replacement. New card skips over this step. Open USBOOT1.7, right-click the mouse and choose run as Administrator. USBOOT1.7 download


v1.70 ▸ USBOOT 1.7
共享 ▾
新建文件夹
名称
修改日期
类型
USBOOT.PAK
2005/4/9 21:30
PAK 文件
USBOOT
2007/2/5 8:44
文本文档
Usboot170
2007/1/23 23:21
应用程序
打开(O)
以管理员身份运行(A)
兼容性疑难解答(Y)

① Run as Administrator

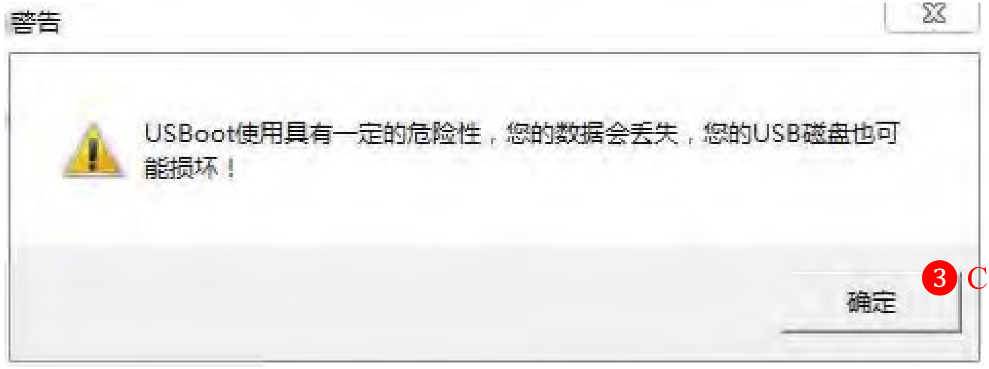

用户帐户控制

您想允许来自未知发布者的以下程序对此计算机进行更改吗?

程序名称: Usboot170.exe
发布者: 未知
文件源: 此计算机上的硬盘驱动器

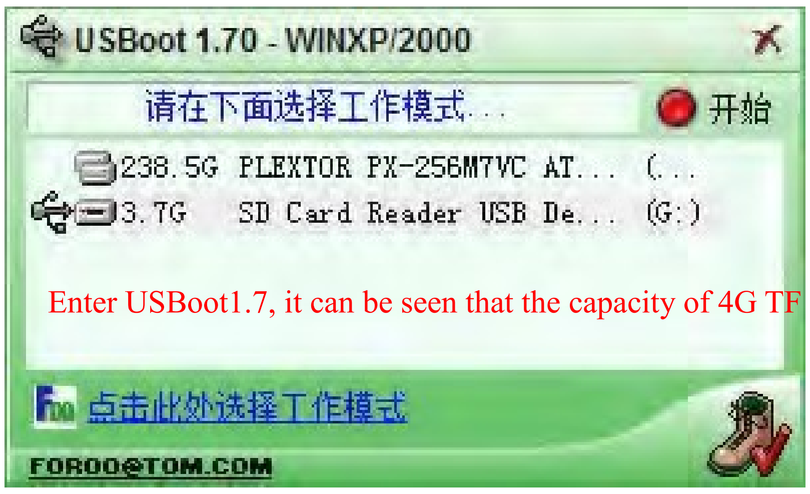
显示详细信息(D)
是(Y)
否(N)
更改这些通知的出现时间

② Choose Yes

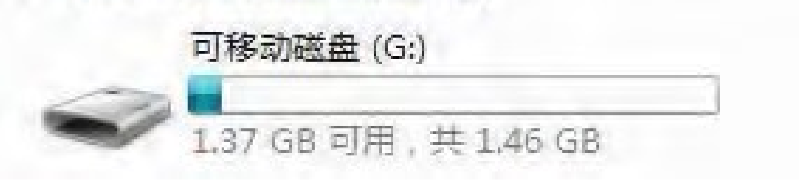


USBoot使用具有一定的危险性，您的数据会丢失，您的USB磁盘也可能损坏！

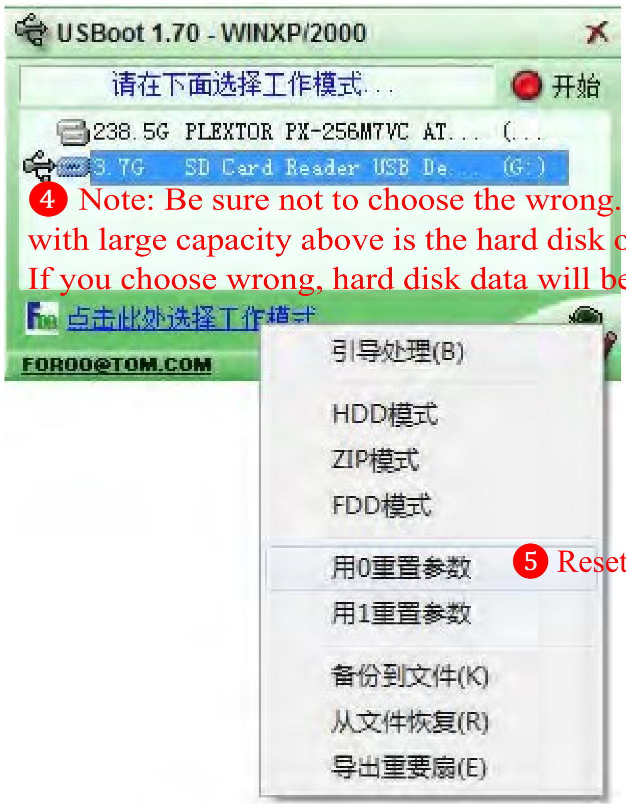
③ Confirm


USBoot 1.70 - WINXP/2000
请在下面选择工作模式...
开始
238.5G PLEXTOR PX-256M7VC AT... (...
3.7G SD Card Reader USB De... (G:)
点击此处选择工作模式
FOROO@TOM.COM

Enter USBoot1.7, it can be seen that the capacity of 4G TF card is 3.7G

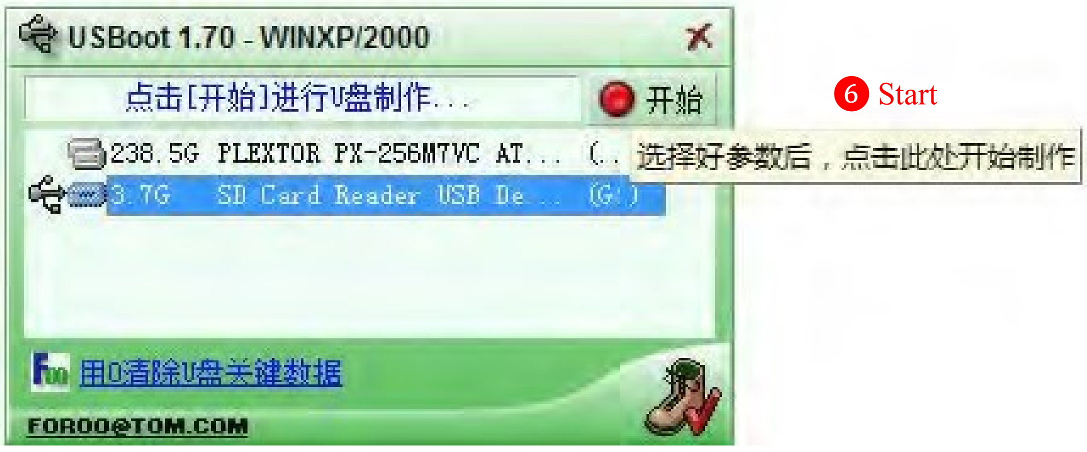

有可移动存储的设备 (1)
可移动磁盘 (G:)
1.37 GB 可用，共 1.46 GB

4G TF card only displays 1.46G in computer

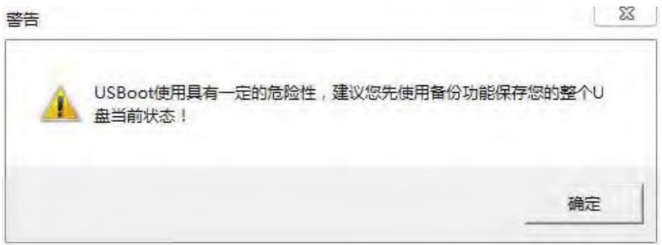

USBoot 1.70 - WINXP/2000
请在下面选择工作模式...
开始
238.5G PLEXTOR PX-256M7VC AT... (...
3.7G SD Card Reader USB De... (G:)
点击此处选择工作模式
FOROO@TOM.COM
引导处理(B)
HDD模式
ZIP模式
FDD模式
用0重置参数
用1重置参数
备份到文件(K)
从文件恢复(R)
导出重要扇(E)

④ Note: Be sure not to choose the wrong. The one with large capacity above is the hard disk of computer. If you choose wrong, hard disk data will be cleared!

⑤ Reset parameter with 0

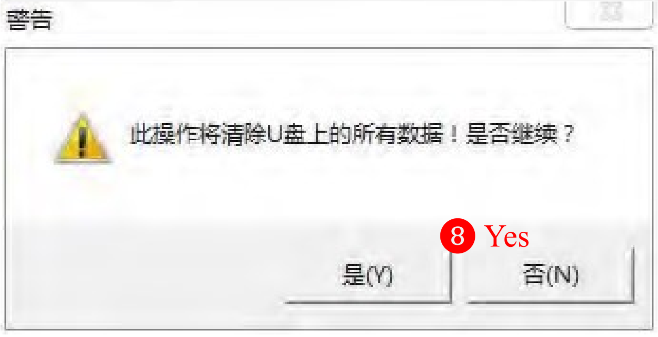

USBoot 1.70 - WINXP/2000
点击[开始]进行U盘制作...
开始
238.5G PLEXTOR PX-256M7VC AT... (...
3.7G SD Card Reader USB De... (G:)
选择好参数后，点击此处开始制作
用0清除U盘关键数据
FOROO@TOM.COM

⑥ Start



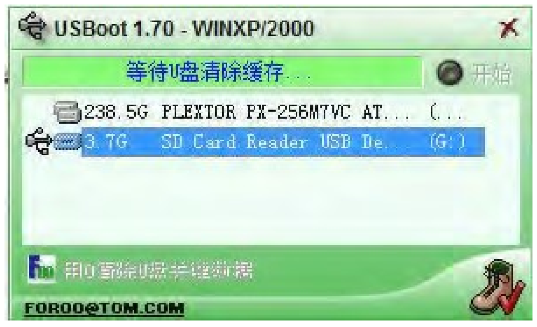
USBoot使用具有一定的危险性，建议您先使用备份功能保存您的整个U盘当前状态！

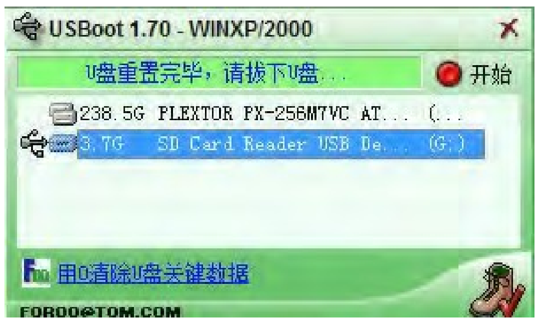
⑦ Confirm

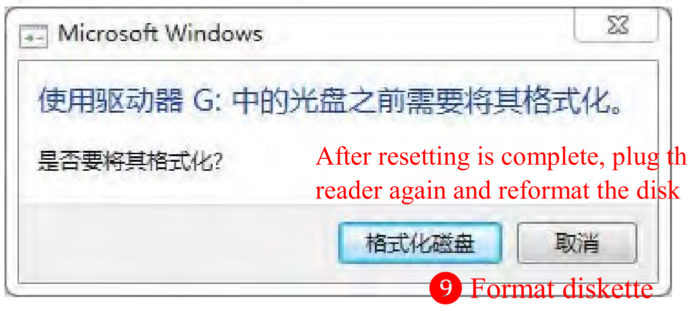


此操作将清除U盘上的所有数据！是否继续？

⑧ Yes


USBoot 1.70 - WINXP/2000
等待U盘清除缓存...
开始
238.5G PLEXTOR PX-256M7VC AT... (...
3.7G SD Card Reader USB De... (G:)
用0清除U盘关键数据
FOROO@TOM.COM


USBoot 1.70 - WINXP/2000
U盘重置完毕，请拔下U盘...
开始
238.5G PLEXTOR PX-256M7VC AT... (...
3.7G SD Card Reader USB De... (G:)
用0清除U盘关键数据
FOROO@TOM.COM


Microsoft Windows

使用驱动器 G: 中的光盘之前需要将其格式化。

是否要将其格式化?

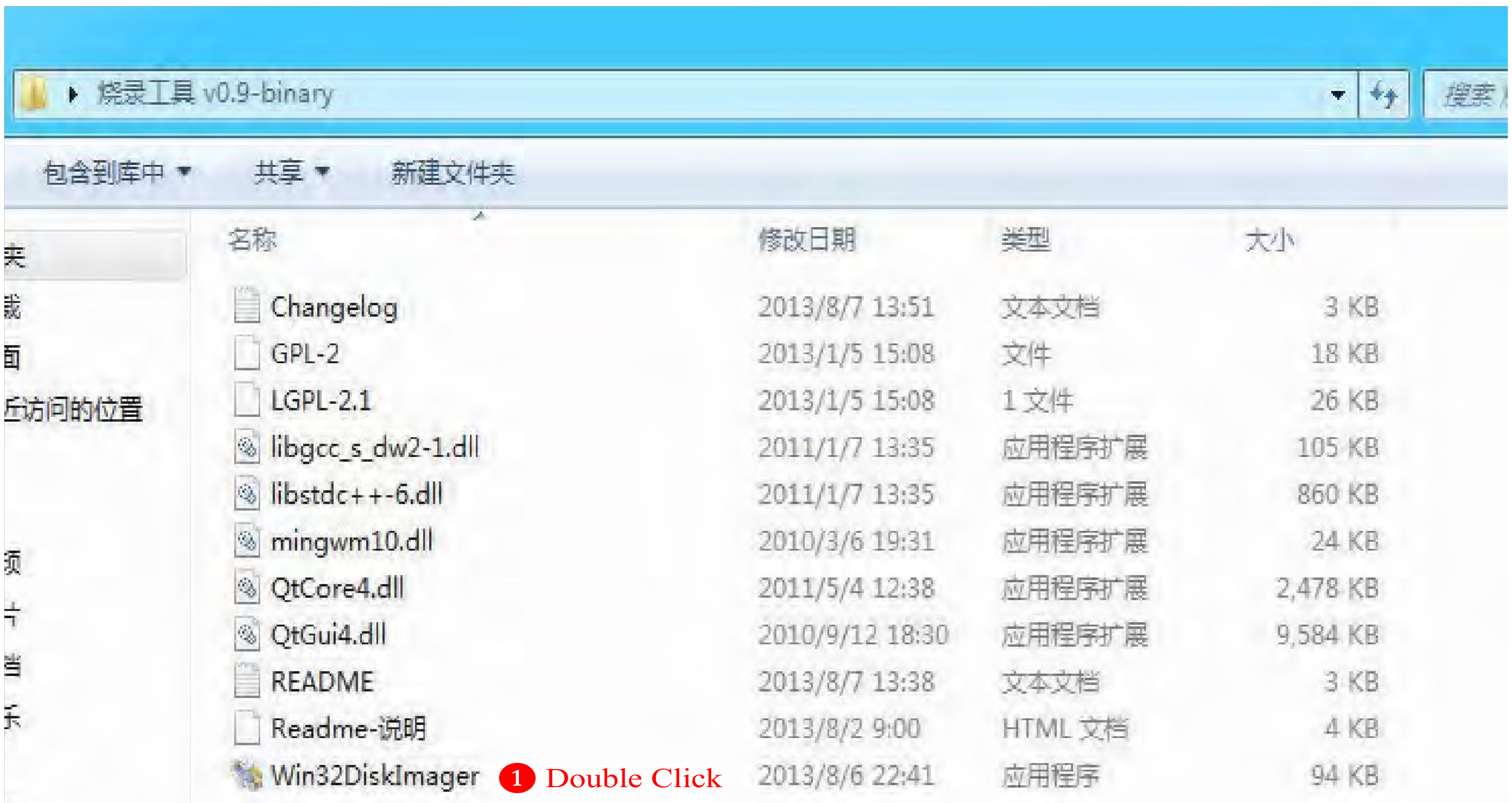
格式化磁盘
取消

After resetting is complete, plug the card reader again and reformat the disk

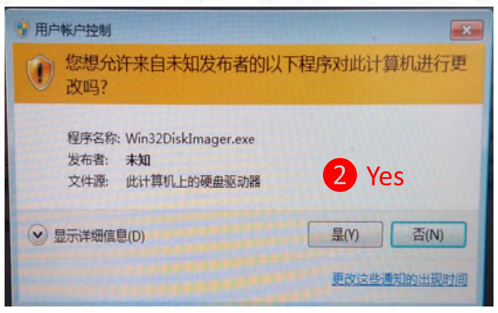
⑨ Format diskette

After completing above 8 steps, just wait. If prompts like “unable to write” appear, please check the 1st step to see whether it is operated correctly

II. Burn-in test program to TF card


烧录工具 v0.9-binary
搜索
包含到库中 ▾
共享 ▾
新建文件夹
最近访问的位置

名称	修改日期	类型	大小
Changelog	2013/8/7 13:51	文本文档	3 KB
GPL-2	2013/1/5 15:08	文件	18 KB
LGPL-2.1	2013/1/5 15:08	1 文件	26 KB
libgcc_s_dw2-1.dll	2011/1/7 13:35	应用程序扩展	105 KB
libstdc++-6.dll	2011/1/7 13:35	应用程序扩展	860 KB
mingwm10.dll	2010/3/6 19:31	应用程序扩展	24 KB
QtCore4.dll	2011/5/4 12:38	应用程序扩展	2,478 KB
QtGui4.dll	2010/9/12 18:30	应用程序扩展	9,584 KB
README	2013/8/7 13:38	文本文档	3 KB
Readme-说明	2013/8/2 9:00	HTML 文档	4 KB
Win32DiskImager ① Double Click	2013/8/6 22:41	应用程序	94 KB

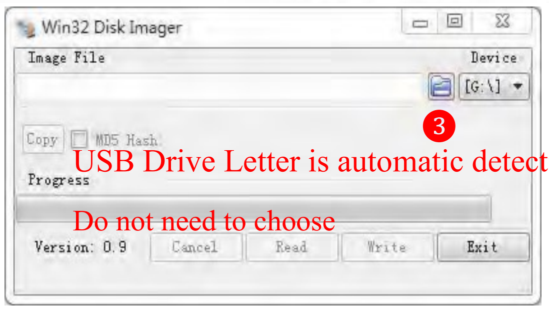

用户帐户控制

您想允许来自未知发布者的以下程序对此计算机进行更改吗?

程序名称: Win32DiskImager.exe
发布者: 未知
文件源: 此计算机上的硬盘驱动器

② Yes

显示详细信息(D)
是(Y)
否(N)
更改这些通知的出现时间

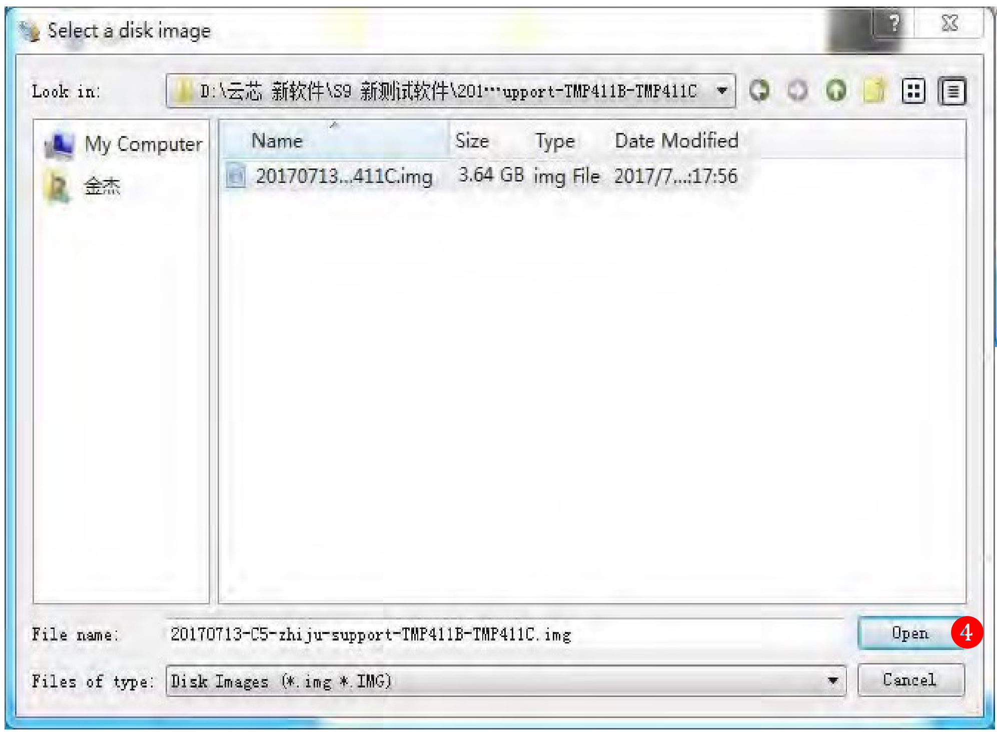

Win32 Disk Imager
Image File
Device
[G:\]
Copy
MD5 Hash
Progress
Version: 0.9
Cancel
Read
Write
Exit

③ USB Drive Letter is automatic detection

Do not need to choose

Find the location of IMG format burning file.

Everyone stores the file in different place, so find it in your own computer.


Select a disk image
My Computer
金杰
Open
Cancel

Look in: D:\云芯 新软件\S9 新测试软件\201…upport-TMP411B-TMP411C

Name	Size	Type	Date Modified
20170713...411C.img	3.64 GB	img File	2017/7,...17:56

File name: 20170713-C5-zhiju-support-TMP411B-TMP411C.img ④

Files of type: Disk Images (*.img *.IMG)

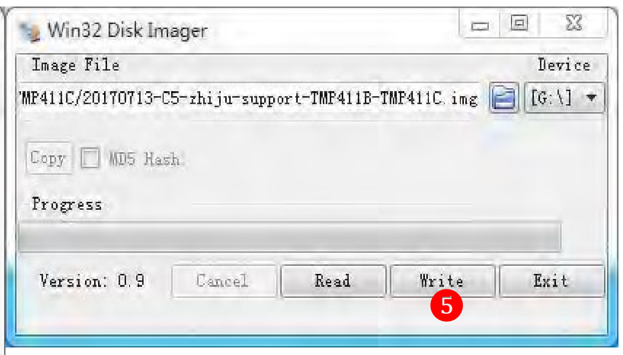
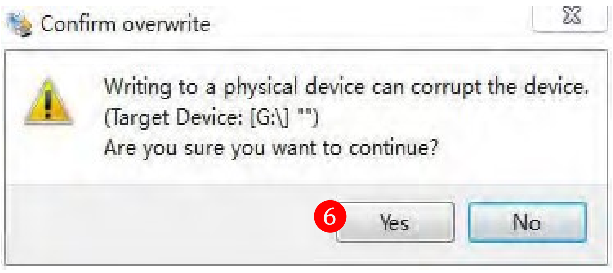

Win32 Disk Imager
Image File
Device
Copy
MD5 Hash
Progress
Version: 0.9
Cancel
Read
Write
Exit

Image File: MP411C/20170713-C5-zhiju-support-TMP411B-TMP411C.img
Device: [G:\]

⑤

Pop up clerk box, and choose YES


Confirm overwrite

Writing to a physical device can corrupt the device.
(Target Device: [G:\] "")
Are you sure you want to continue?

⑥ Yes No

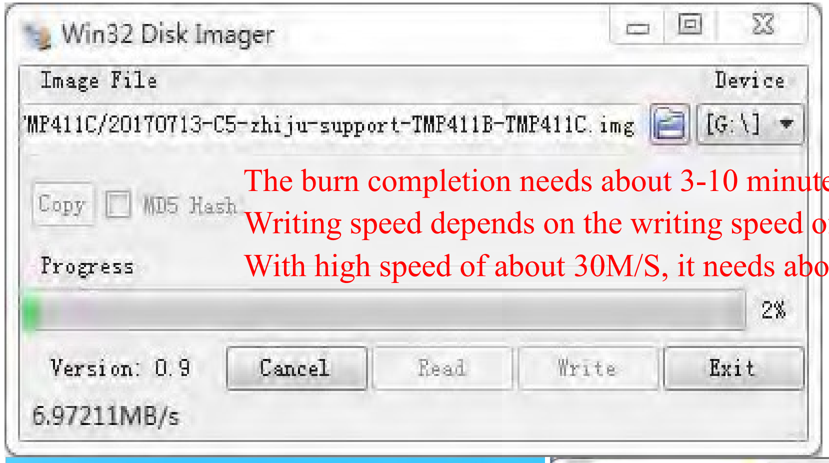
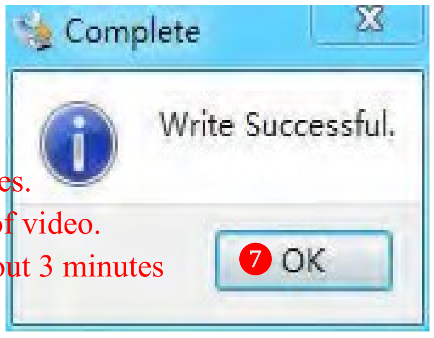

Win32 Disk Imager
Image File
Device
Copy
MD5 Hash
Progress
Cancel
Read
Write
Exit

Image File: MP411C/20170713-C5-zhiju-support-TMP411B-TMP411C.img
Device: [G:\]
Progress: 2%
Version: 0.9
6.97211MB/s

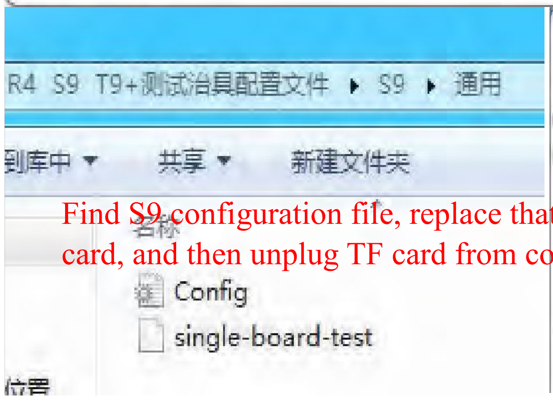
The burn completion needs about 3-10 minutes.
Writing speed depends on the writing speed of video.
With high speed of about 30M/S, it needs about 3 minutes



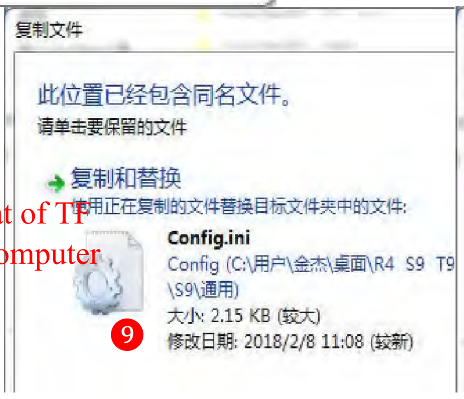
Write Successful.

⑦ OK

After burn completion, click OK, and close burning software.


R4 S9 T9+测试治具配置文件 ▸ S9 ▸ 通用
到库中 ▾
共享 ▾
新建文件夹
名称
Config
single-board-test
位置

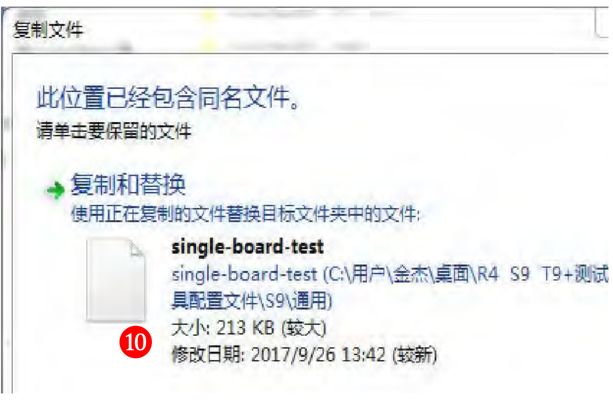
Find S9 configuration file, replace that of TF card, and then unplug TF card from computer



此位置已经包含同名文件。
请单击要保留的文件

复制和替换
使用正在复制的文件替换目标文件夹中的文件:

Config.ini
Config (C:\用户\金杰\桌面\R4 S9 T9 \S9\通用)
大小: 2.15 KB (较大)
修改日期: 2018/2/8 11:08 (较新)
⑨



此位置已经包含同名文件。
请单击要保留的文件

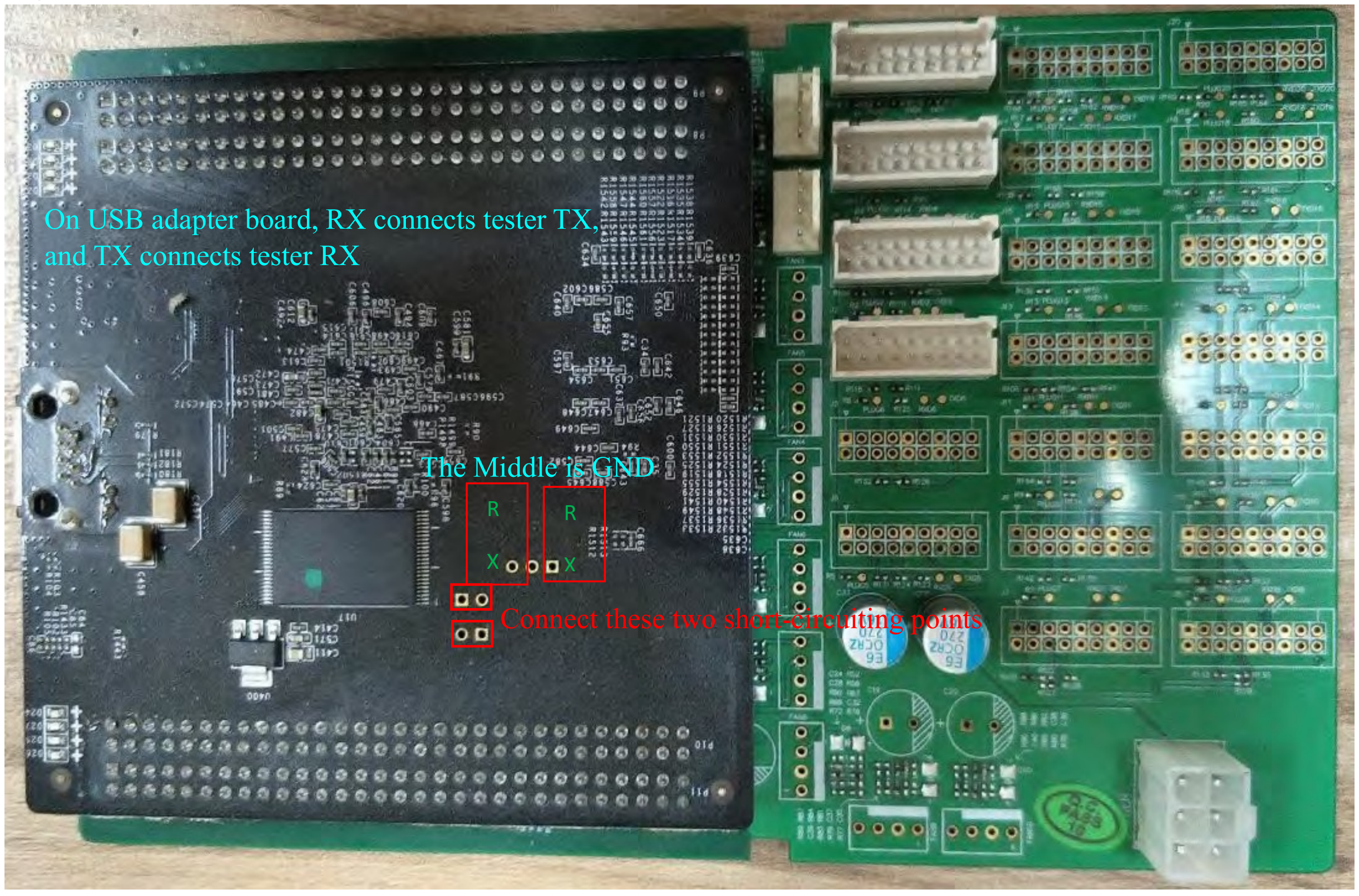
复制和替换
使用正在复制的文件替换目标文件夹中的文件:

single-board-test
single-board-test (C:\用户\金杰\桌面\R4 S9 T9+测试具配置文件\S9\通用)
大小: 213 KB (较大)
修改日期: 2017/9/26 13:42 (较新)
⑩

7. Single Board Test

I. Insert the TF card with burned test program to the TF card slot of hashboard tester

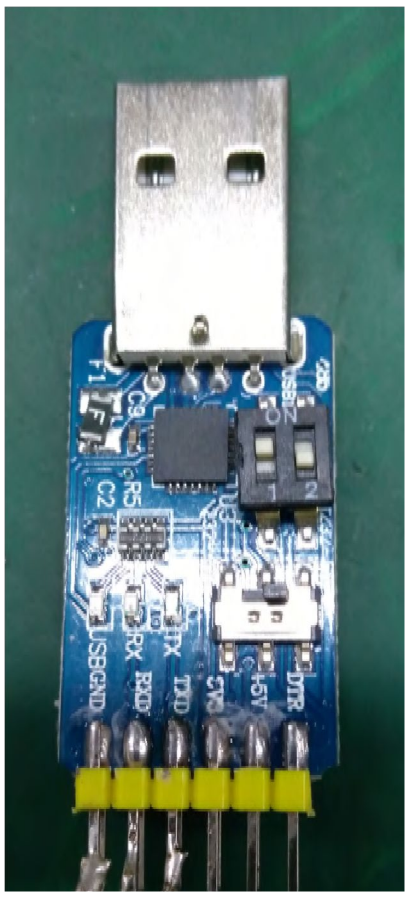
II. Transfer USB to TTL adapter board via drop-out line and weld to hashboard tester. The specific connection methods see below figure.



On USB adapter board, RX connects tester TX, and TX connects tester RX

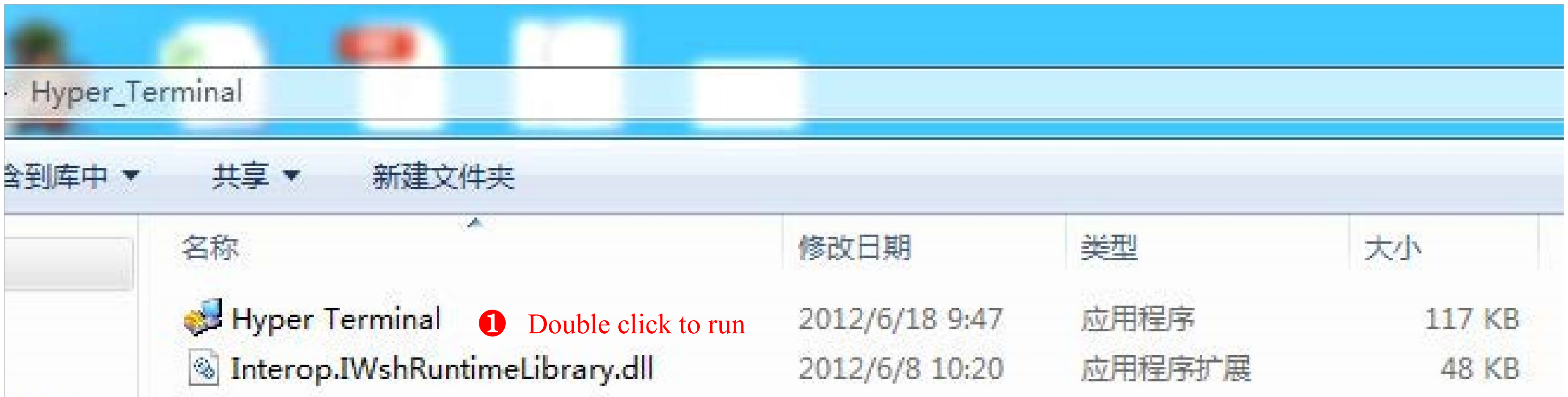
The Middle is GND

Connect these two short-circuiting points



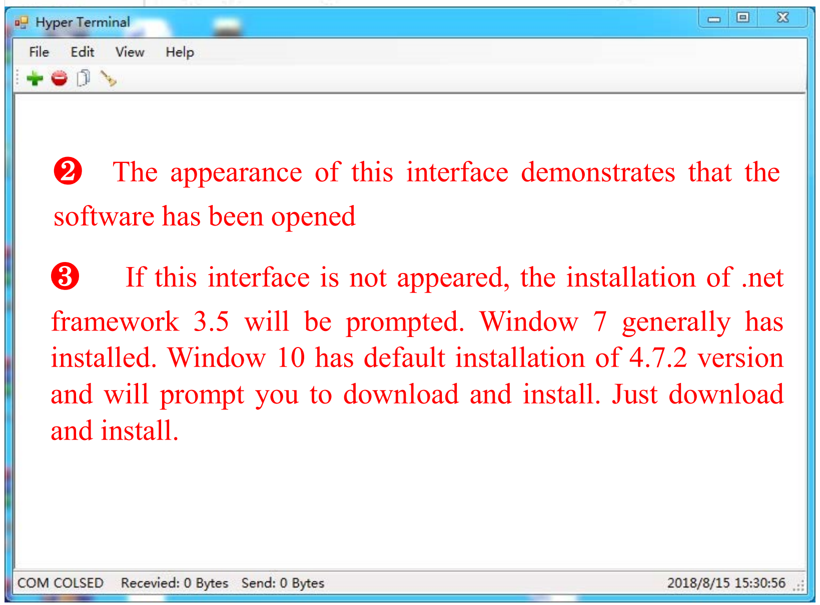
III. Install the drive to transfer USB to TTL in computer, and then transfer USB to TTL adapter board and insert to computer USB interface. PL2303 drive download CP 2102 drive download, open Hyper Terminal directory.

V. Run Hyper Terminal and ensure your computer has installed .net framework 3.5. If .net framework 3.5has not been installed, Window 10 will promote you to download and install.



名称	修改日期	类型	大小
Hyper Terminal	2012/6/18 9:47	应用程序	117 KB
Interop.IWshRuntimeLibrary.dll	2012/6/8 10:20	应用程序扩展	48 KB

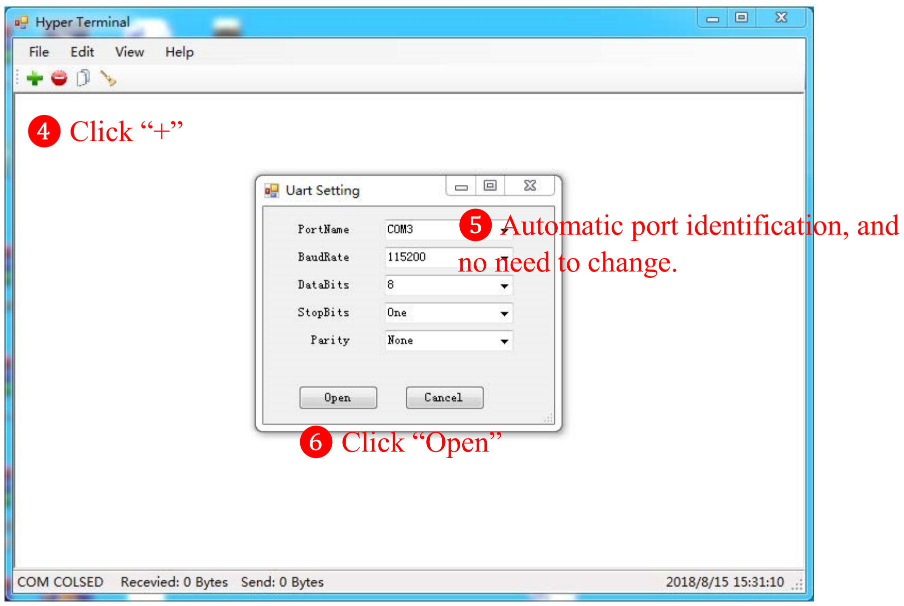
❶ Double click to run



❷ The appearance of this interface demonstrates that the software has been opened

❸ If this interface is not appeared, the installation of .net framework 3.5 will be prompted. Window 7 generally has installed. Window 10 has default installation of 4.7.2 version and will prompt you to download and install. Just download and install.

COM COLSED Recevied: 0 Bytes Send: 0 Bytes 2018/8/15 15:30:56



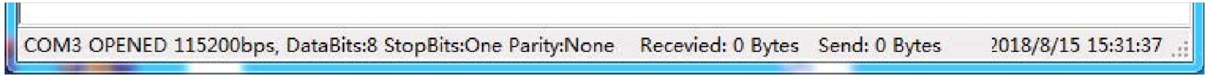
❹ Click "+"

PortName COM3
BaudRate 115200
DataBits 8
StopBits One
Parity None

❺ Automatic port identification, and no need to change.

❻ Click "Open"

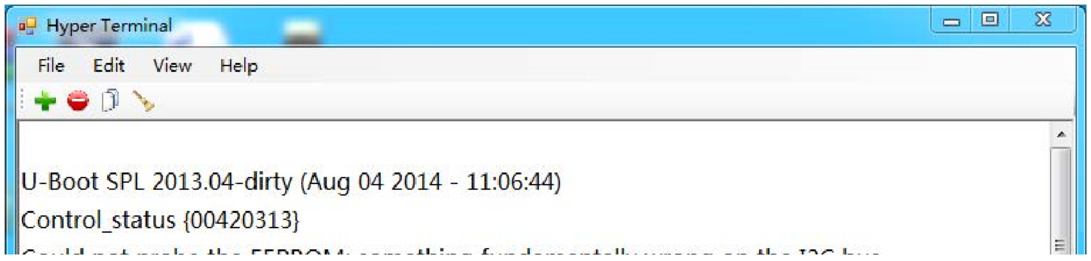
COM COLSED Recevied: 0 Bytes Send: 0 Bytes 2018/8/15 15:31:10



COM3 OPENED 115200bps, DataBits:8 StopBits:One Parity:None Recevied: 0 Bytes Send: 0 Bytes 2018/8/15 15:31:37

❼ The display of "COM3 Opened" demonstrates successful connection

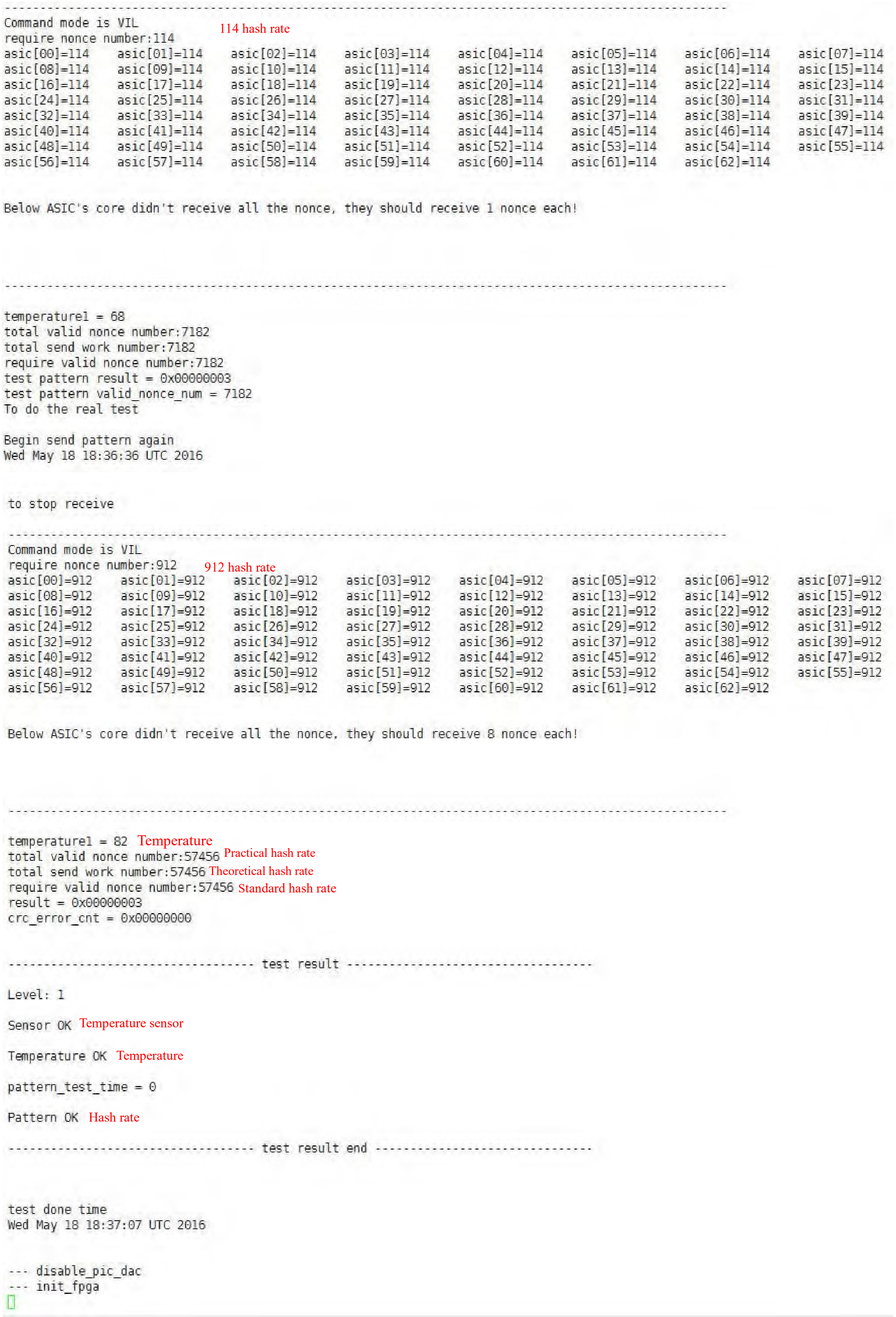
VI. Power on the hashboard tester and wait, until hashboard tester screen appears test program information; connect the IO mouth drop-out line of hashboard and power cord, and then press test key to test.



```
U-Boot SPL 2013.04-dirty (Aug 04 2014 - 11:06:44)
Control_status {00420313}
```

V. Fault Maintenance

●(I) Troubleshooting of Single Board:

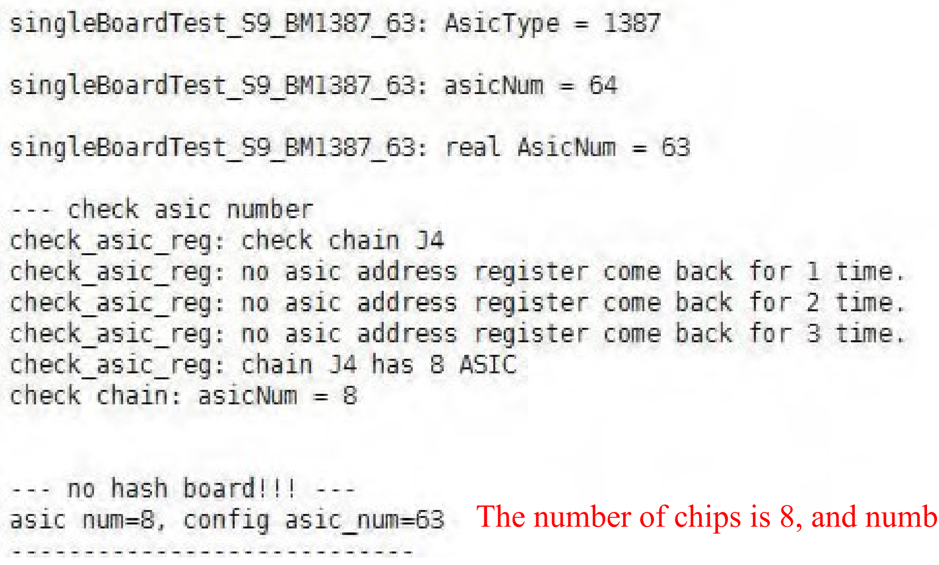


```
----------------------------------------------------------------------------------------------------
Command mode is VIL
require nonce number:114
asic[00]=114    asic[01]=114    asic[02]=114    asic[03]=114    asic[04]=114    asic[05]=114    asic[06]=114    asic[07]=114
asic[08]=114    asic[09]=114    asic[10]=114    asic[11]=114    asic[12]=114    asic[13]=114    asic[14]=114    asic[15]=114
asic[16]=114    asic[17]=114    asic[18]=114    asic[19]=114    asic[20]=114    asic[21]=114    asic[22]=114    asic[23]=114
asic[24]=114    asic[25]=114    asic[26]=114    asic[27]=114    asic[28]=114    asic[29]=114    asic[30]=114    asic[31]=114
asic[32]=114    asic[33]=114    asic[34]=114    asic[35]=114    asic[36]=114    asic[37]=114    asic[38]=114    asic[39]=114
asic[40]=114    asic[41]=114    asic[42]=114    asic[43]=114    asic[44]=114    asic[45]=114    asic[46]=114    asic[47]=114
asic[48]=114    asic[49]=114    asic[50]=114    asic[51]=114    asic[52]=114    asic[53]=114    asic[54]=114    asic[55]=114
asic[56]=114    asic[57]=114    asic[58]=114    asic[59]=114    asic[60]=114    asic[61]=114    asic[62]=114


Below ASIC's core didn't receive all the nonce, they should receive 1 nonce each!




----------------------------------------------------------------------------------------------------

temperature1 = 68
total valid nonce number:7182
total send work number:7182
require valid nonce number:7182
test pattern result = 0x00000003
test pattern valid_nonce_num = 7182
To do the real test

Begin send pattern again
Wed May 18 18:36:36 UTC 2016


 to stop receive

----------------------------------------------------------------------------------------------------
Command mode is VIL
require nonce number:912
asic[00]=912    asic[01]=912    asic[02]=912    asic[03]=912    asic[04]=912    asic[05]=912    asic[06]=912    asic[07]=912
asic[08]=912    asic[09]=912    asic[10]=912    asic[11]=912    asic[12]=912    asic[13]=912    asic[14]=912    asic[15]=912
asic[16]=912    asic[17]=912    asic[18]=912    asic[19]=912    asic[20]=912    asic[21]=912    asic[22]=912    asic[23]=912
asic[24]=912    asic[25]=912    asic[26]=912    asic[27]=912    asic[28]=912    asic[29]=912    asic[30]=912    asic[31]=912
asic[32]=912    asic[33]=912    asic[34]=912    asic[35]=912    asic[36]=912    asic[37]=912    asic[38]=912    asic[39]=912
asic[40]=912    asic[41]=912    asic[42]=912    asic[43]=912    asic[44]=912    asic[45]=912    asic[46]=912    asic[47]=912
asic[48]=912    asic[49]=912    asic[50]=912    asic[51]=912    asic[52]=912    asic[53]=912    asic[54]=912    asic[55]=912
asic[56]=912    asic[57]=912    asic[58]=912    asic[59]=912    asic[60]=912    asic[61]=912    asic[62]=912


Below ASIC's core didn't receive all the nonce, they should receive 8 nonce each!




----------------------------------------------------------------------------------------------------

temperature1 = 82
total valid nonce number:57456
total send work number:57456
require valid nonce number:57456
result = 0x00000003
crc_error_cnt = 0x00000000


---------------------------------- test result ----------------------------------

Level: 1

Sensor OK

Temperature OK

pattern_test_time = 0

Pattern OK

---------------------------------- test result end ------------------------------


test done time
Wed May 18 18:37:07 UTC 2016


--- disable_pic_dac
--- init_fpga
```

Test results of normal single board

Common Faults in Single Board Test:

1. The Missing of Chip and the Report of Numerical Number



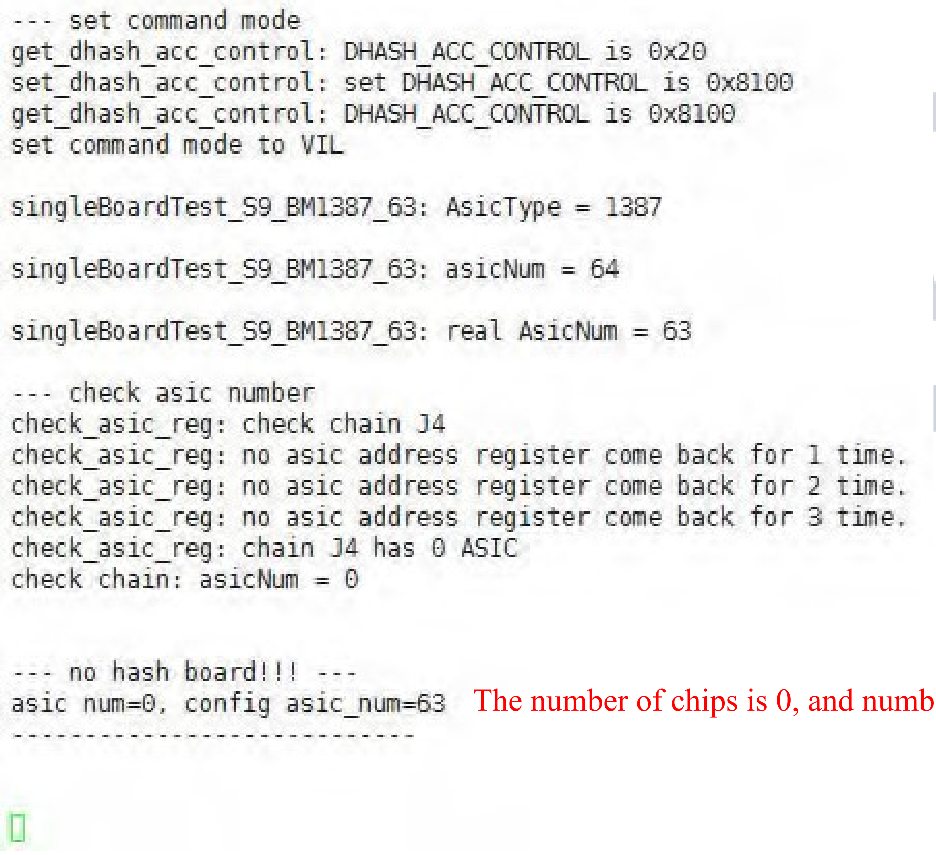
```
singleBoardTest_S9_BM1387_63: AsicType = 1387

singleBoardTest_S9_BM1387_63: asicNum = 64

singleBoardTest_S9_BM1387_63: real AsicNum = 63

--- check asic number
check_asic_reg: check chain J4
check_asic_reg: no asic address register come back for 1 time.
check_asic_reg: no asic address register come back for 2 time.
check_asic_reg: no asic address register come back for 3 time.
check_asic_reg: chain J4 has 8 ASIC
check chain: asicNum = 8


--- no hash board!!! ---
asic num=8, config asic_num=63
----------------------------
```

The number of chips is 8, and number of configuration chips is 63

The complete machine configures 63 chips, but only 8 chips have been detected in single board test.

Under this circumstance, first test whether CO voltage is normal. The fastest way is short circuit to the CO ground of chip 8, press test key and begin to test. If it still reports 8, continue short circuit to the CO ground of chip 9. If it still reports when short circuit to chip 9, this means chip 9 works abnormally. Measure the voltages and resistances of chip 7, 8 and 9, and find abnormal chip to replace (in most cases, report 8 is caused by the anomaly of chip 9). If report 7 when short circuit to 8, this indicates the anomaly of previous chip, maintain in the same way.

2. The Missing of Chip and the Report of 0



```
--- set command mode
get_dhash_acc_control: DHASH_ACC_CONTROL is 0x20
set_dhash_acc_control: set DHASH_ACC_CONTROL is 0x8100
get_dhash_acc_control: DHASH_ACC_CONTROL is 0x8100
set command mode to VIL

singleBoardTest_S9_BM1387_63: AsicType = 1387

singleBoardTest_S9_BM1387_63: asicNum = 64

singleBoardTest_S9_BM1387_63: real AsicNum = 63

--- check asic number
check_asic_reg: check chain J4
check_asic_reg: no asic address register come back for 1 time.
check_asic_reg: no asic address register come back for 2 time.
check_asic_reg: no asic address register come back for 3 time.
check_asic_reg: chain J4 has 0 ASIC
check chain: asicNum = 0


--- no hash board!!! ---
asic num=0, config asic_num=63
----------------------------
```

The number of chips is 0, and number of configuration chips is 63

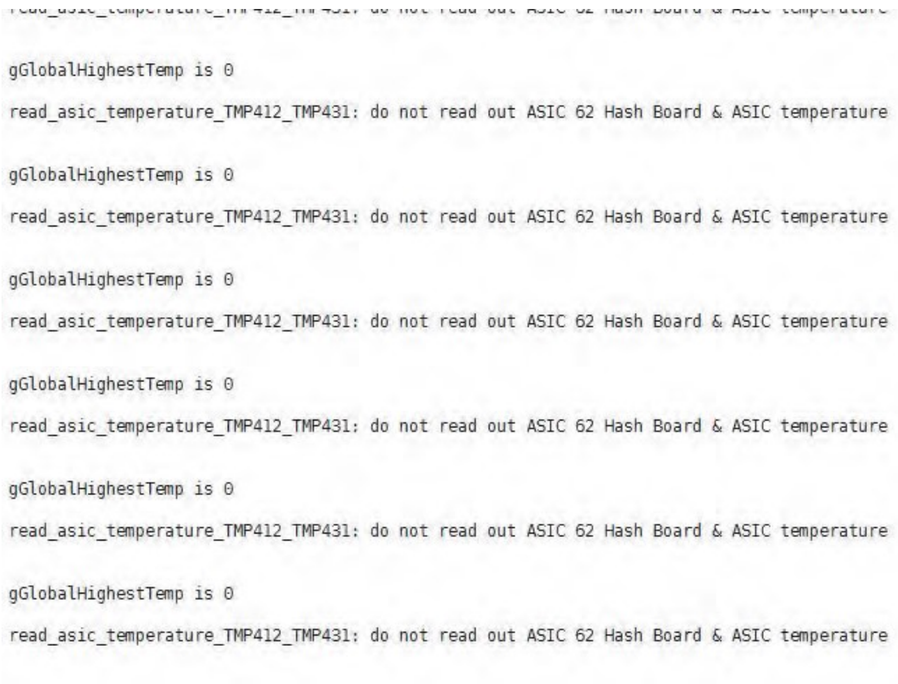
The situation of reporting 0 is caused by the anomaly of RX signal, and there are three common situations

❶ All of the 5 test points of 63 chips have no voltage or only the last 5 voltage domains have voltage. This situation is caused by that power supply works abnormally (directly measure whether there is about 8.4V voltage between the cooling fins on the back of the first and the last voltage domains.). Test whether the first and last pin of U1 are short circuit, whether 4 MOS tubes are short circuit, and then replace it in the event of short circuit. If there is no short circuit, exchange with PIC chip on good board. The rise of voltage means the missing of PIC software, burn original PIC software, and burning method sees PIC burning instruction.

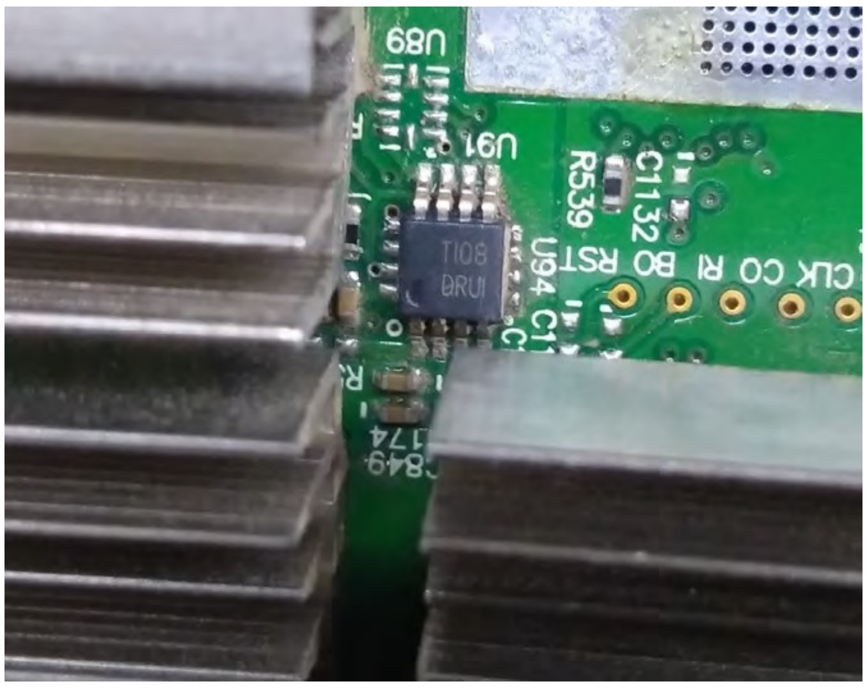
❷ If voltages of all of the 5 test points of 63 chips are normal, test whether the voltage of each pin of Q86 of 1.9 version or U88 of 4.2 version is normal. If any problem is detected, use the material of good board to replace. If ok, mean that exactly this component has problem; if not ok, replace No. 1 computing chip

❸ The RO voltage anomaly of some chips is the most common situation. RO signal transmits from back to front, replace the chip after the place where RO voltage is abnormal.

3. Unable to Detect Temperature



```
gGlobalHighestTemp is 0

read_asic_temperature_TMP412_TMP431: do not read out ASIC 62 Hash Board & ASIC temperature

gGlobalHighestTemp is 0

read_asic_temperature_TMP412_TMP431: do not read out ASIC 62 Hash Board & ASIC temperature

gGlobalHighestTemp is 0

read_asic_temperature_TMP412_TMP431: do not read out ASIC 62 Hash Board & ASIC temperature

gGlobalHighestTemp is 0

read_asic_temperature_TMP412_TMP431: do not read out ASIC 62 Hash Board & ASIC temperature

gGlobalHighestTemp is 0

read_asic_temperature_TMP412_TMP431: do not read out ASIC 62 Hash Board & ASIC temperature

gGlobalHighestTemp is 0

read_asic_temperature_TMP412_TMP431: do not read out ASIC 62 Hash Board & ASIC temperature
```



In this situation, firstly check the model of the temperature sensor IC beside chip 62 as above Fig, to ensure the consistency of the temperature configuration file in hashboard tester TF card and the temperature sensor IC model of tested board. If they are inconsistent, replace temperature configuration file and use tester to have a power-on test again.

If the temperature configuration file is correct, replace chip 62 (if the replacement of chip 62 of 1.9 version is noneffective, take the computing chip 46, 25 and 2 on I² bus wire into account)

S9 common temperature configuration file

The hashboard of dual temperature sensor has only 1 configuration file below 3.9 version.

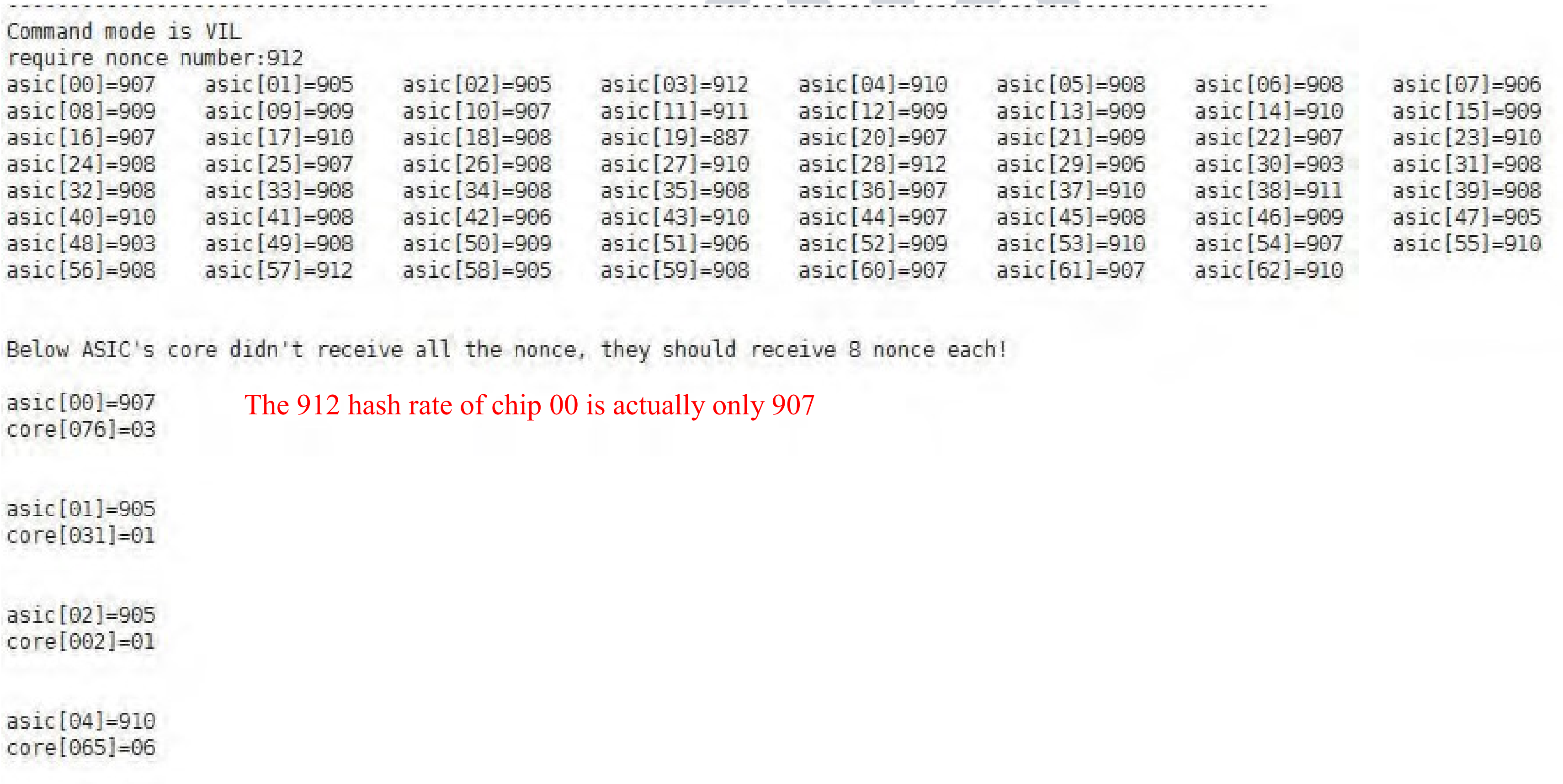
The temperature sensors of TMP451, TMP461, TMP421, TMP431 and ECT218 use the same configuration file, and the external appearance is QFN package square IC.

The two temperature sensors of DRU1 and 411B use the same configuration profile, and the appearance sees above Fig.

411C uses a separate configuration file, and the appearance is the same as that of DRU1

Distinguish model according to the words on IC surface: TMP451, TMP461, TMP421, TMP431 and ECT218 are usually in U89, and DRU1, 411B and 411C are usually in U91

4. Low Hashing

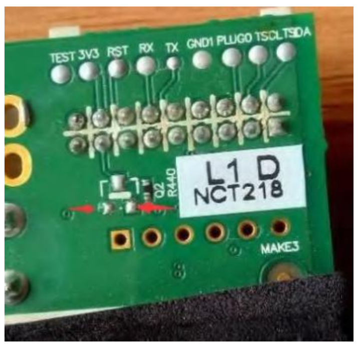


```
--------------------------------------------------------------------------------
Command mode is VIL
require nonce number:912
asic[00]=907    asic[01]=905    asic[02]=905    asic[03]=912    asic[04]=910    asic[05]=908    asic[06]=908    asic[07]=906
asic[08]=909    asic[09]=909    asic[10]=907    asic[11]=911    asic[12]=909    asic[13]=909    asic[14]=910    asic[15]=909
asic[16]=907    asic[17]=910    asic[18]=908    asic[19]=887    asic[20]=907    asic[21]=909    asic[22]=907    asic[23]=910
asic[24]=908    asic[25]=907    asic[26]=908    asic[27]=910    asic[28]=912    asic[29]=906    asic[30]=903    asic[31]=908
asic[32]=908    asic[33]=908    asic[34]=908    asic[35]=908    asic[36]=907    asic[37]=910    asic[38]=911    asic[39]=908
asic[40]=910    asic[41]=908    asic[42]=906    asic[43]=910    asic[44]=907    asic[45]=908    asic[46]=909    asic[47]=905
asic[48]=903    asic[49]=908    asic[50]=909    asic[51]=906    asic[52]=909    asic[53]=910    asic[54]=907    asic[55]=910
asic[56]=908    asic[57]=912    asic[58]=905    asic[59]=908    asic[60]=907    asic[61]=907    asic[62]=910

Below ASIC's core didn't receive all the nonce, they should receive 8 nonce each!

asic[00]=907
core[076]=03


asic[01]=905
core[031]=01


asic[02]=905
core[002]=01


asic[04]=910
core[065]=06
```

The 912 hash rate of chip 00 is actually only 907

114 and 912 hash rate: all that are unable to reach standard hash rate will display chip number and the actual hash rate below, and the gap should not be far. In the situation that several chips of low hashing appear, replace the chip with the lowest hash rate, and then test again. If there is still chip with very low hash rate, replace this chip with lowest hash rate and then test again.

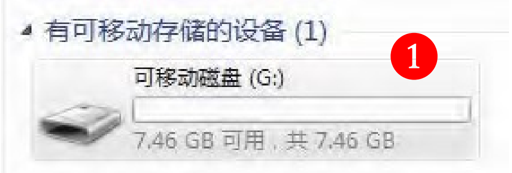
5. When single board test of 4.21 version and above is OK, all the hash rate will be 0 in complete machine test

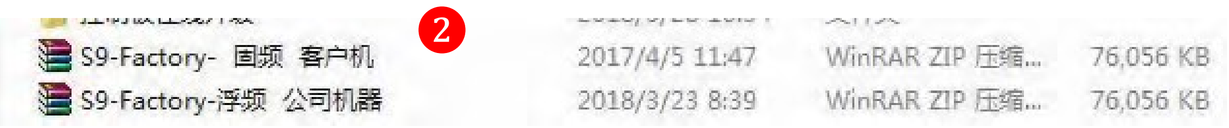


Add an IUF 0603 capacitor between pin 1 and pin 2 of O2 on the back of IO Mouth

(II) The Upgrade of Control Panel T Card

1. Upgrade Card Making

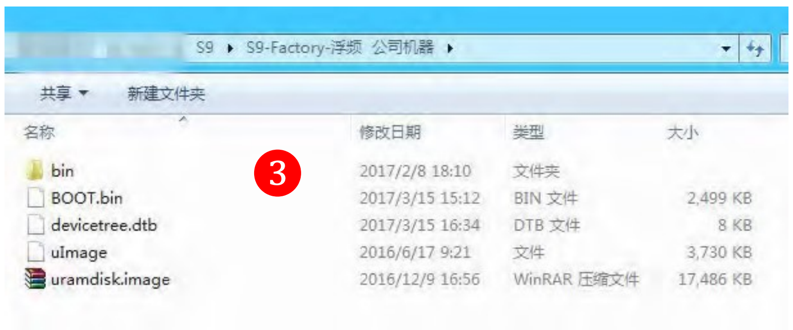




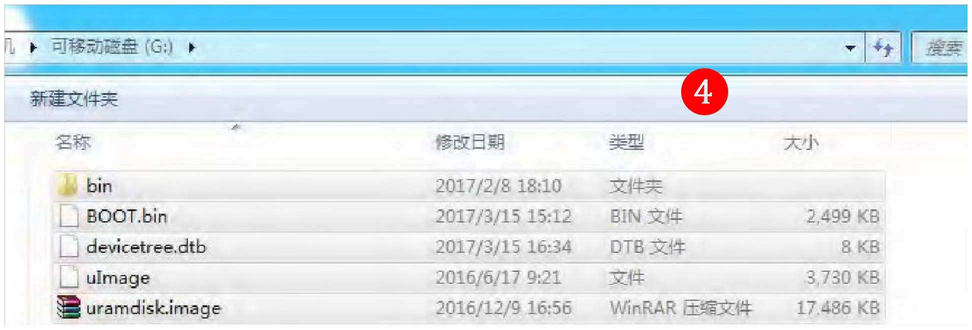
S9-Factory- 固频 客户机	2017/4/5 11:47	WinRAR ZIP 压缩...	76,056 KB
S9-Factory-浮频 公司机器	2018/3/23 8:39	WinRAR ZIP 压缩...	76,056 KB

① Find a blank TF card (it must be a blank card; if card has content, format firstly; if capacity is abnormal, restore the capacity and then format).

② Find the location of the download upgrade file in computer and decompress it.



名称	修改日期	类型	大小
bin	2017/2/8 18:10	文件夹	
BOOT.bin	2017/3/15 15:12	BIN 文件	2,499 KB
devicetree.dtb	2017/3/15 16:34	DTB 文件	8 KB
uImage	2016/6/17 9:21	文件	3,730 KB
uramdisk.image	2016/12/9 16:56	WinRAR 压缩文件	17,486 KB



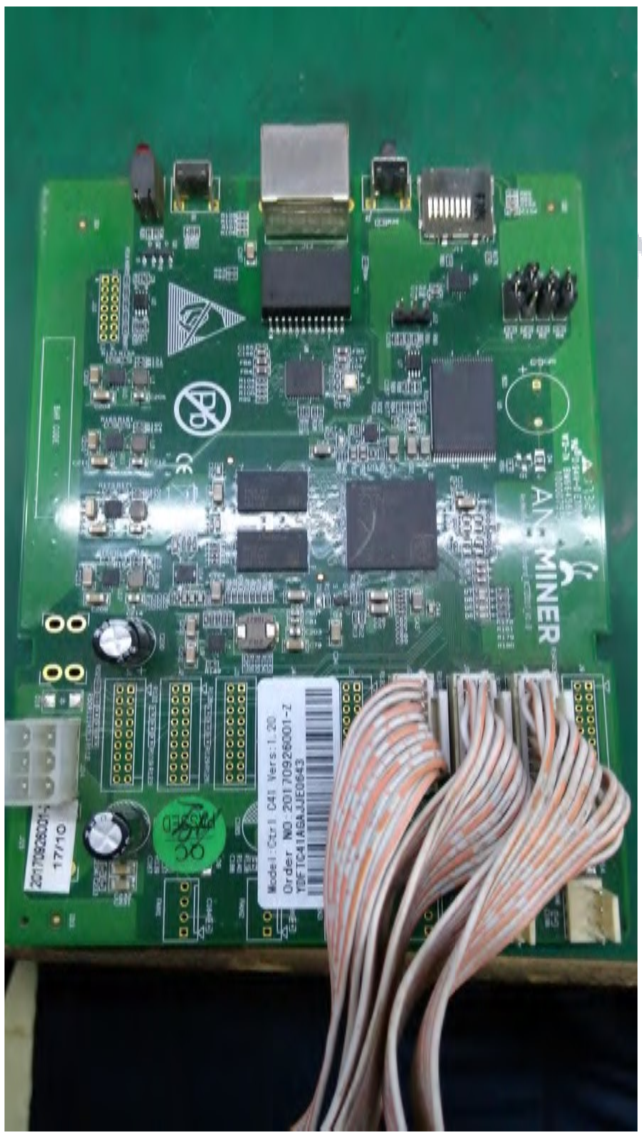
名称	修改日期	类型	大小
bin	2017/2/8 18:10	文件夹	
BOOT.bin	2017/3/15 15:12	BIN 文件	2,499 KB
devicetree.dtb	2017/3/15 16:34	DTB 文件	8 KB
uImage	2016/6/17 9:21	文件	3,730 KB
uramdisk.image	2016/12/9 16:56	WinRAR 压缩文件	17,486 KB

③ The file after decompression

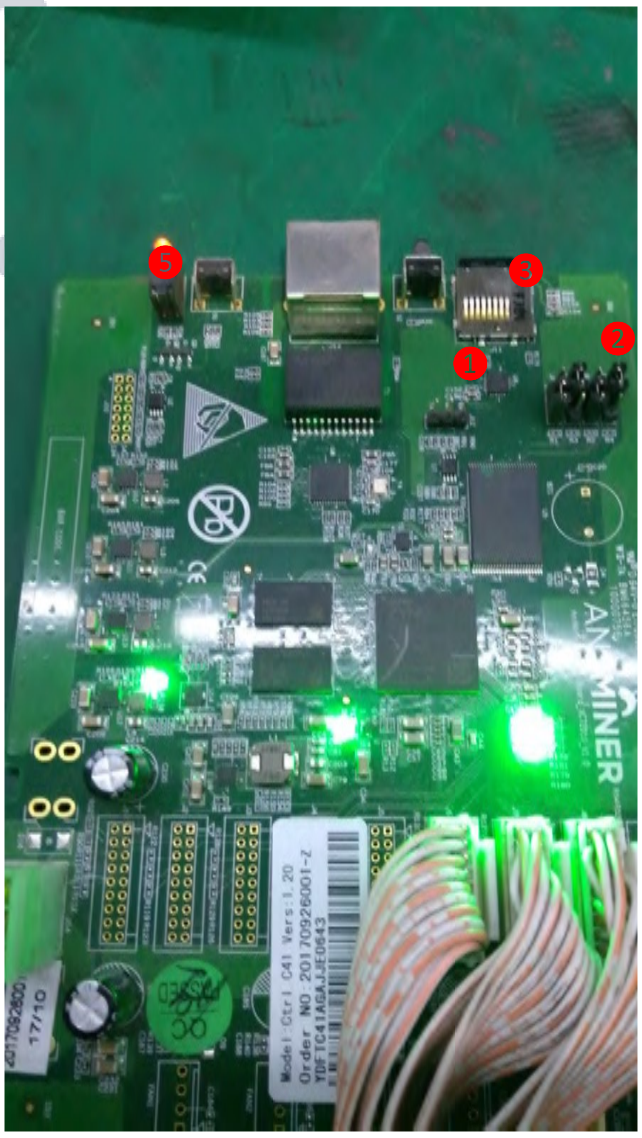
④ Copy all the decompression file to TF card

2. Upgrade

ATA
NT TRAINING A



The state before upgrade and after upgrade in need of recovery



In the process of upgrade

❶Firstly check whether the IC beside TF card slot has material. If empty, find material handler and repair welding after receiving material.

❷ Jump the jumper cap on the edge to the side of card slot (JP4)

❸ Insert TF card with upgrade software

❹ Power on

❺ Wait for upgrade. When the upgrade is successful, red light and green light begin to flash incessantly. The process needs about 1 minute, and too short time indicates abnormal upgrade

❻ Power off

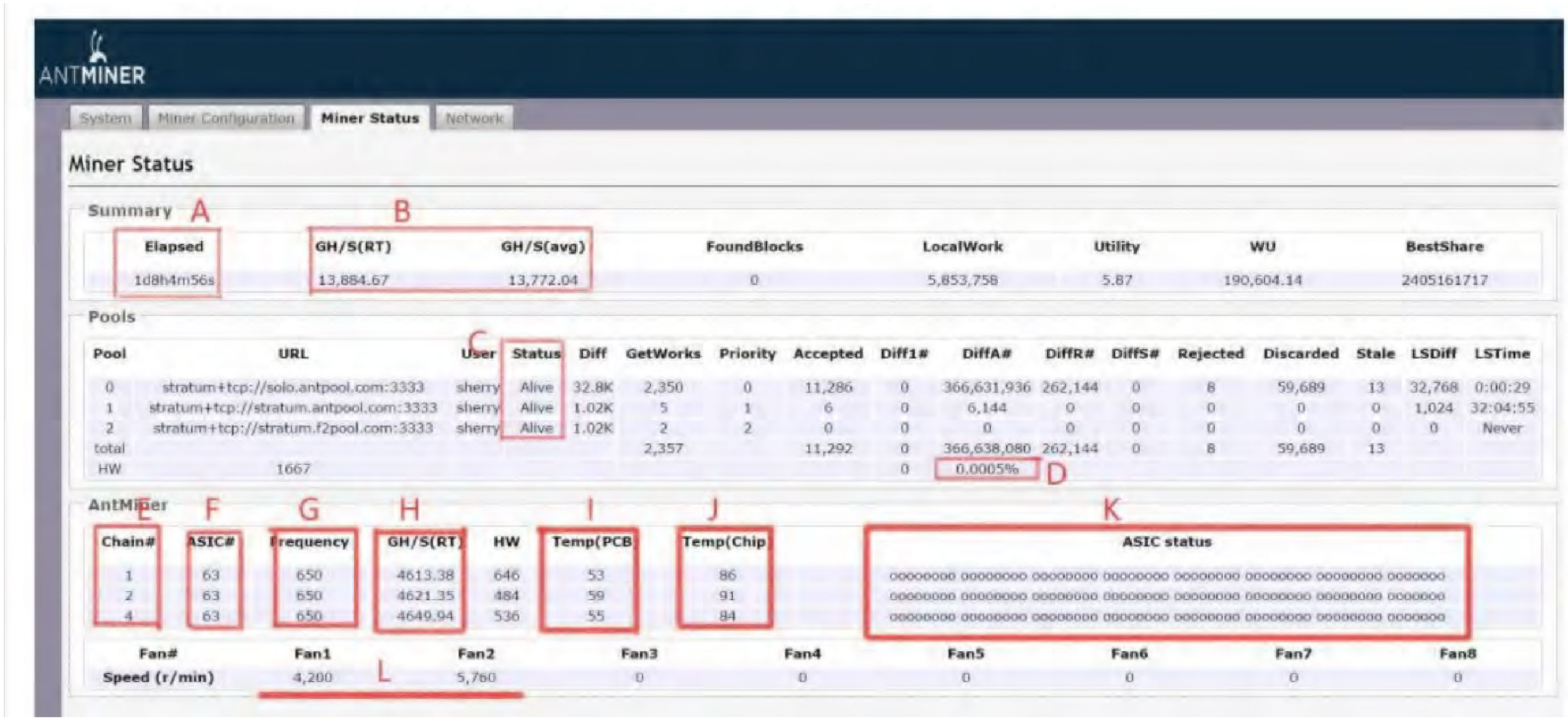
❼ Unplug TF card

❽ Jump the jumper cap to home position, complete the upgrade

The hash rate of the machine that TF card has swiped will decline due to underclocking, so online upgrade is a must to restore original hash rate

(III). Troubleshooting of Complete Machine

A: service hours B: hash rate of miner C: the status of mining pool, alive means connecting D: error rate: not more than 0.03% normally
E: the serial number of hashboard F: the number of chips G: running frequency H: hash rate of single hashboard
I: the temperature of hashboard J: the temperature of chip K: the status of chip (appear X or - means anomaly)
L: the rotating speed of two fans
HW: the number of hardware errors, this needs no attention. Only see the error rate of D. Pay attention to error rate rather than specific data



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
1d8h4m56s	13,884.67	13,772.04	0	5,853,758	5.87	190,604.14	2405161717

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime
0	stratum+tcp://solo.antpool.com:3333	sherry	Alive	32.8K	2,350	0	11,286	0	366,631,936	262,144	0	8	59,689	13	32,768	0:00:29
1	stratum+tcp://stratum.antpool.com:3333	sherry	Alive	1.02K	5	1	6	0	6,144	0	0	0	0	0	1,024	32:04:55
2	stratum+tcp://stratum.f2pool.com:3333	sherry	Alive	1.02K	2	2	0	0	0	0	0	0	0	0	0	Never
total					2,357		11,292	0	366,638,080	262,144	0	8	59,689	13		
HW	1667							0	0.0005%							

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB	Temp(Chip	ASIC status
1	63	650	4613.38	646	53	86	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
2	63	650	4621.35	484	59	91	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
4	63	650	4649.94	536	55	84	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo

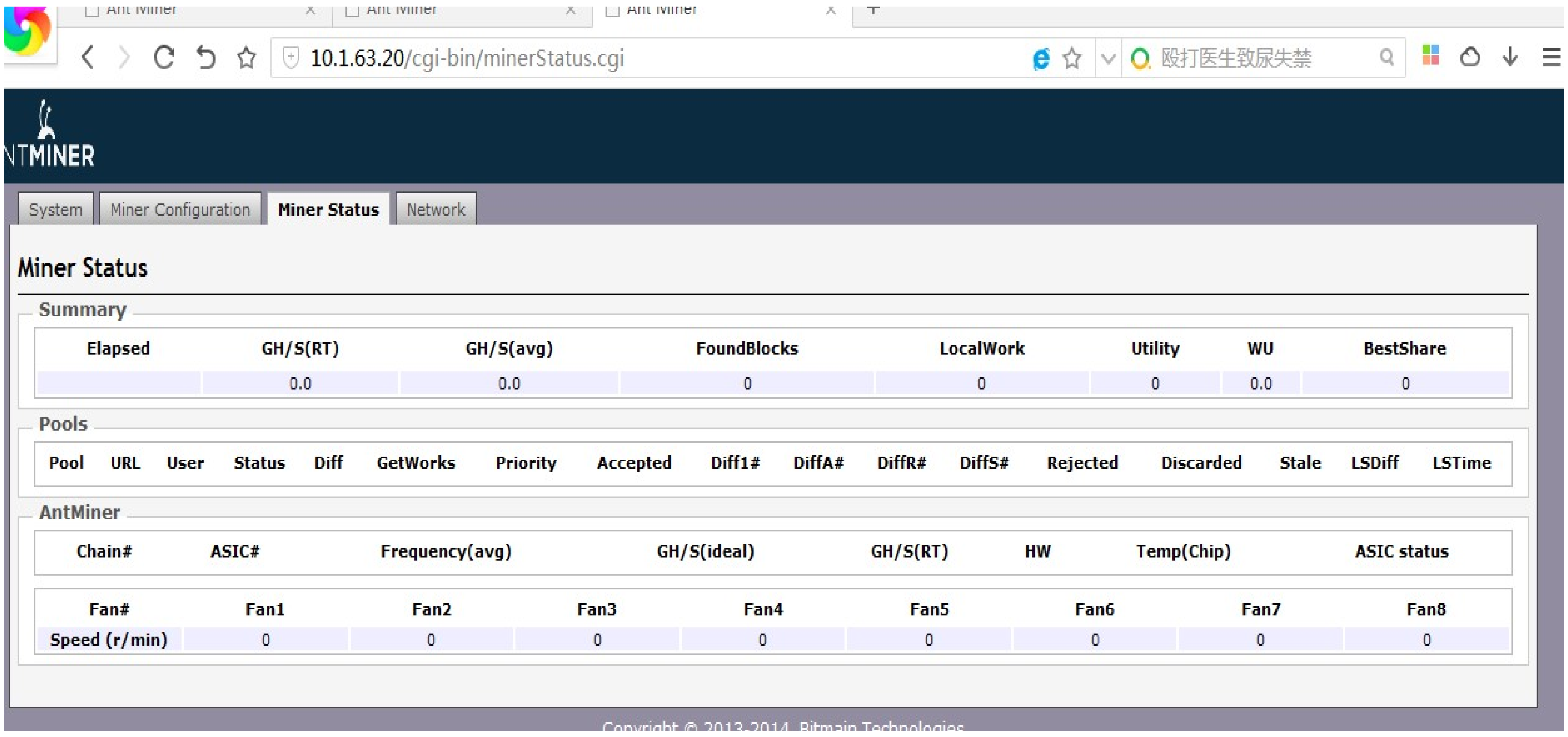
Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	4,200	5,760	0	0	0	0	0	0

The interface of background web page

1. Log in monitoring interface (WEB). This type of malfunction is mainly caused by the fault of hashboard, and seldom is caused by operation environment, fan, external network, firmware, etc.

The following is the solutions to all kinds of common phenomena:

1) No configuration information on hash rate interface. See below Fig 22:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
	0.0	0.0	0	0	0	0.0	0

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime

AntMiner

Chain#	ASIC#	Frequency(avg)	GH/S(ideal)	GH/S(RT)	HW	Temp(Chip)	ASIC status

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	0	0	0	0	0	0

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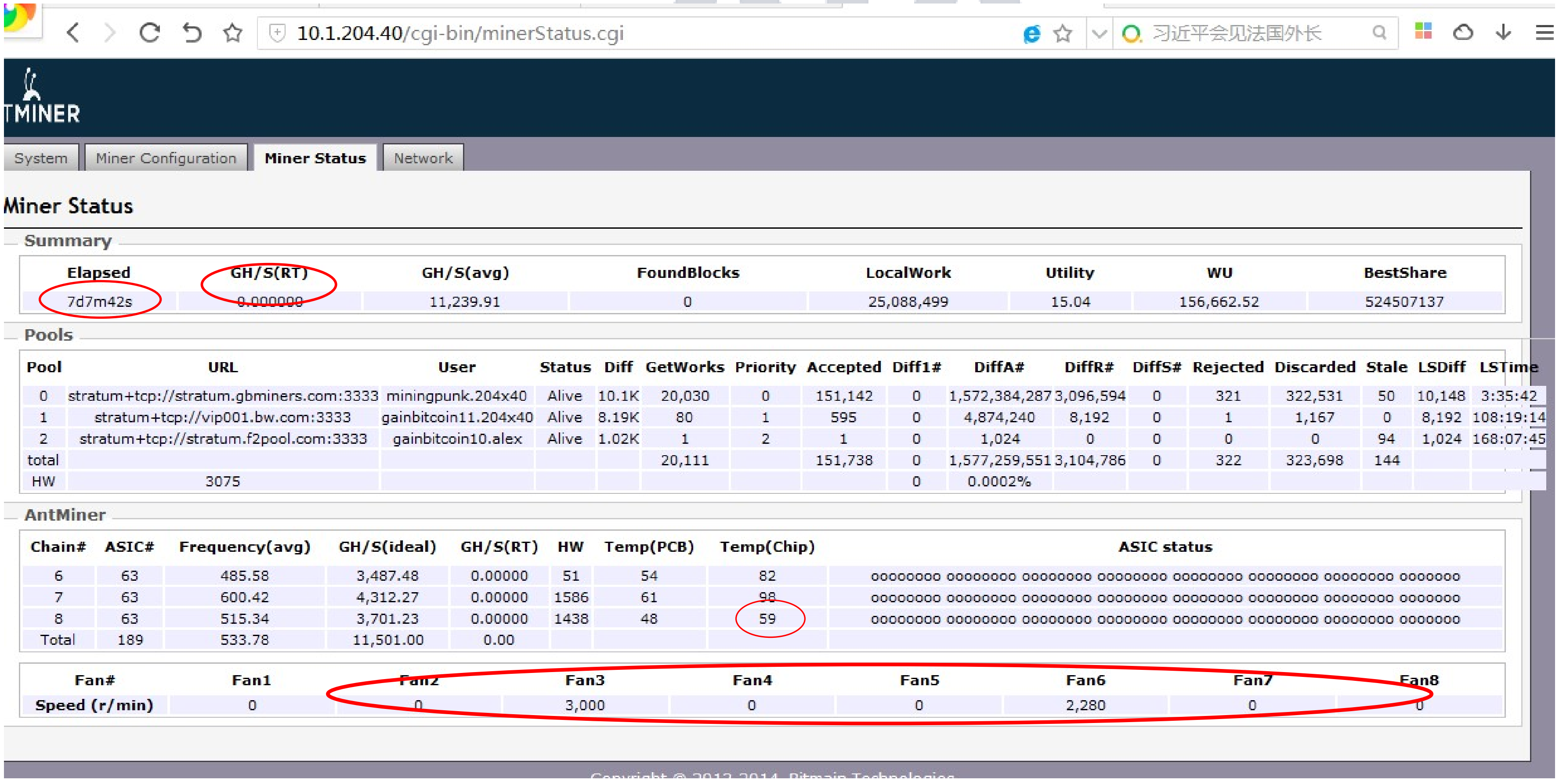
Fig 22. The Screenshot of No Configuration Information

Solution:

- Firstly check the indicator light of miner. If the red status light of miner blinks, the miner is in abnormal status. Check the network of miner. Plug the network cable of miner to computer, PIN the pool of miner, to see whether can get through.
- If indicator light is in normal status, it is most likely that all of the 3 hashboards of miner have problem, such as the rewritten of miner's PIC voltage.
- With regard to the damage of miner's firmware, upgrade the firmware to the latest version through upgrade interface.

2) No GH/S(RT) hash rate, red light blinks. See below Fig 23:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
7d7m42s	0.000000	11,239.91	0	25,088,499	15.04	156,662.52	524507137

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime
0	stratum+tcp://stratum.gbminers.com:3333	miningpunk.204x40	Alive	10.1K	20,030	0	151,142	0	1,572,384,287	3,096,594	0	321	322,531	50	10,148	3:35:42
1	stratum+tcp://vip001.bw.com:3333	gainbitcoin11.204x40	Alive	8.19K	80	1	595	0	4,874,240	8,192	0	1	1,167	0	8,192	108:19:14
2	stratum+tcp://stratum.f2pool.com:3333	gainbitcoin10.alex	Alive	1.02K	1	2	1	0	1,024	0	0	0	0	94	1,024	168:07:45
total					20,111		151,738	0	1,577,259,551	3,104,786	0	322	323,698	144		
HW	3075							0	0.0002%							

AntMiner

Chain#	ASIC#	Frequency(avg)	GH/S(ideal)	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
6	63	485.58	3,487.48	0.00000	51	54	82	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
7	63	600.42	4,312.27	0.00000	1586	61	98	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
8	63	515.34	3,701.23	0.00000	1438	48	59	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
Total	189	533.78	11,501.00	0.00				

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	3,000	0	0	2,280	0	0

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Fig 23. No Hash Rate

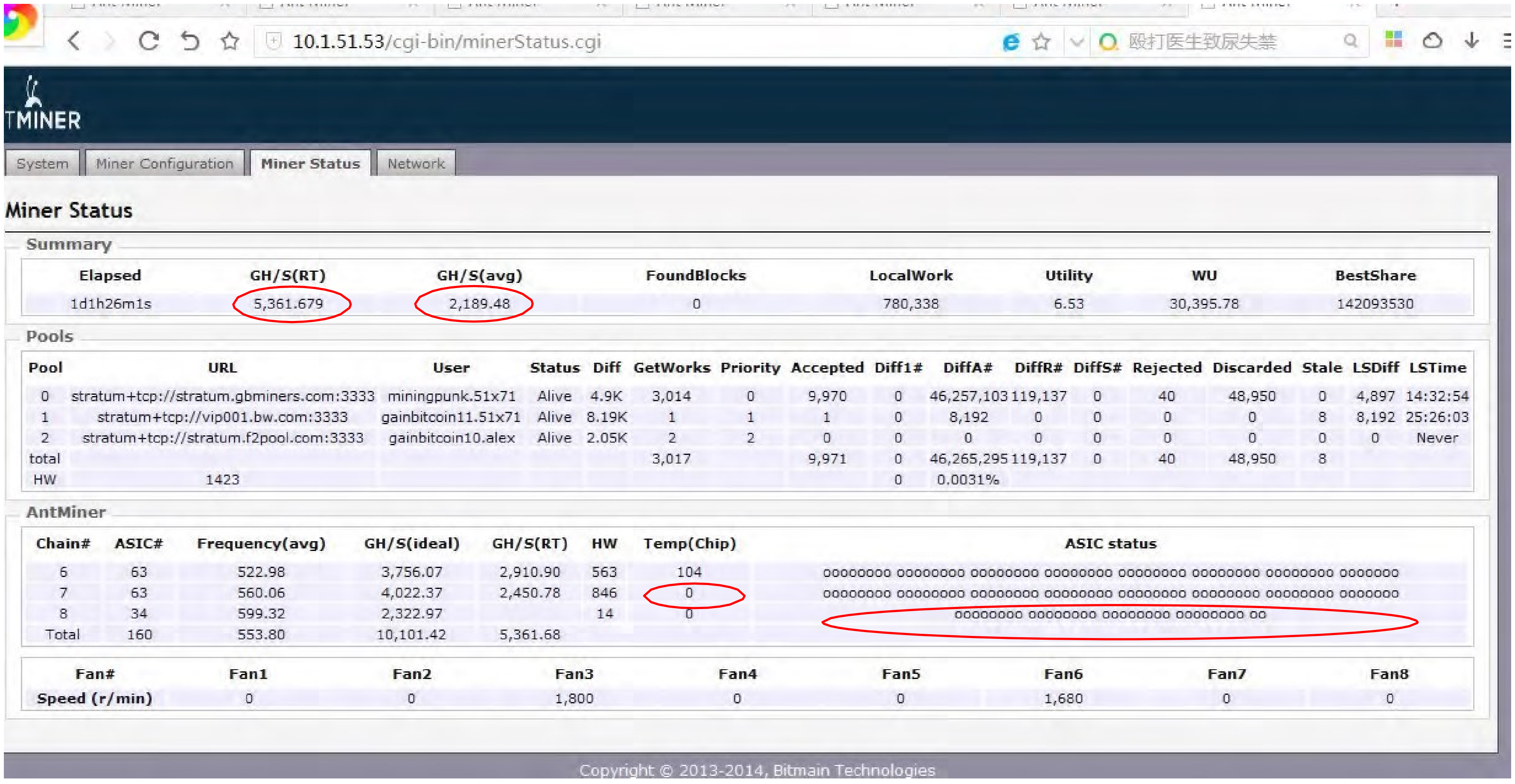
In above phenomenon, miner has operated for 7 days, and GH/S (AVG) has not dropped too much. This indicates the miner has not gone wrong before long. The speed of dual fan is very low and the TEMP (CHIP) of No. 8 board is very low. It is thus clear that the board fell out shortly before, so reboot miner will be OK. This phenomenon closely connects miner's operation environment, especially environmental temperature; for instance, in northern winter, this is very probable to happen in sudden cooling.

In addition, check the network between miner and pool. Unstable external network will also cause this situation.

If reboot cannot make it return to normal, use test tool to give single board test to miner's three hashboards, to check whether hashboard is normal.

Besides, update firmware to the latest version.

3) Line drops, board lacks, or chip drops. See below Fig 24, Fig 25, Fig 26:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
1d1h26m1s	5,361.679	2,189.48	0	780,338	6.53	30,395.78	142093530

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime
0	stratum+tcp://stratum.gbminers.com:3333	miningpunk.51x71	Alive	4.9K	3,014	0	9,970	0	46,257,103	119,137	0	40	48,950	0	4,897	14:32:54
1	stratum+tcp://vip001.bw.com:3333	gainbitcoin11.51x71	Alive	8.19K	1	1	1	0	8,192	0	0	0	0	8	8,192	25:26:03
2	stratum+tcp://stratum.f2pool.com:3333	gainbitcoin10.alex	Alive	2.05K	2	2	0	0	0	0	0	0	0	0	0	Never
total					3,017		9,971	0	46,265,295	119,137	0	40	48,950	8		
HW	1423							0	0.0031%							

AntMiner

Chain#	ASIC#	Frequency(avg)	GH/S(ideal)	GH/S(RT)	HW	Temp(Chip)	ASIC status
6	63	522.98	3,756.07	2,910.90	563	104	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
7	63	560.06	4,022.37	2,450.78	846	0	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
8	34	599.32	2,322.97		14	0	oooooooo oooooooo oooooooo oooooooo oo
Total	160	553.80	10,101.42	5,361.68			

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	1,800	0	0	1,680	0	0

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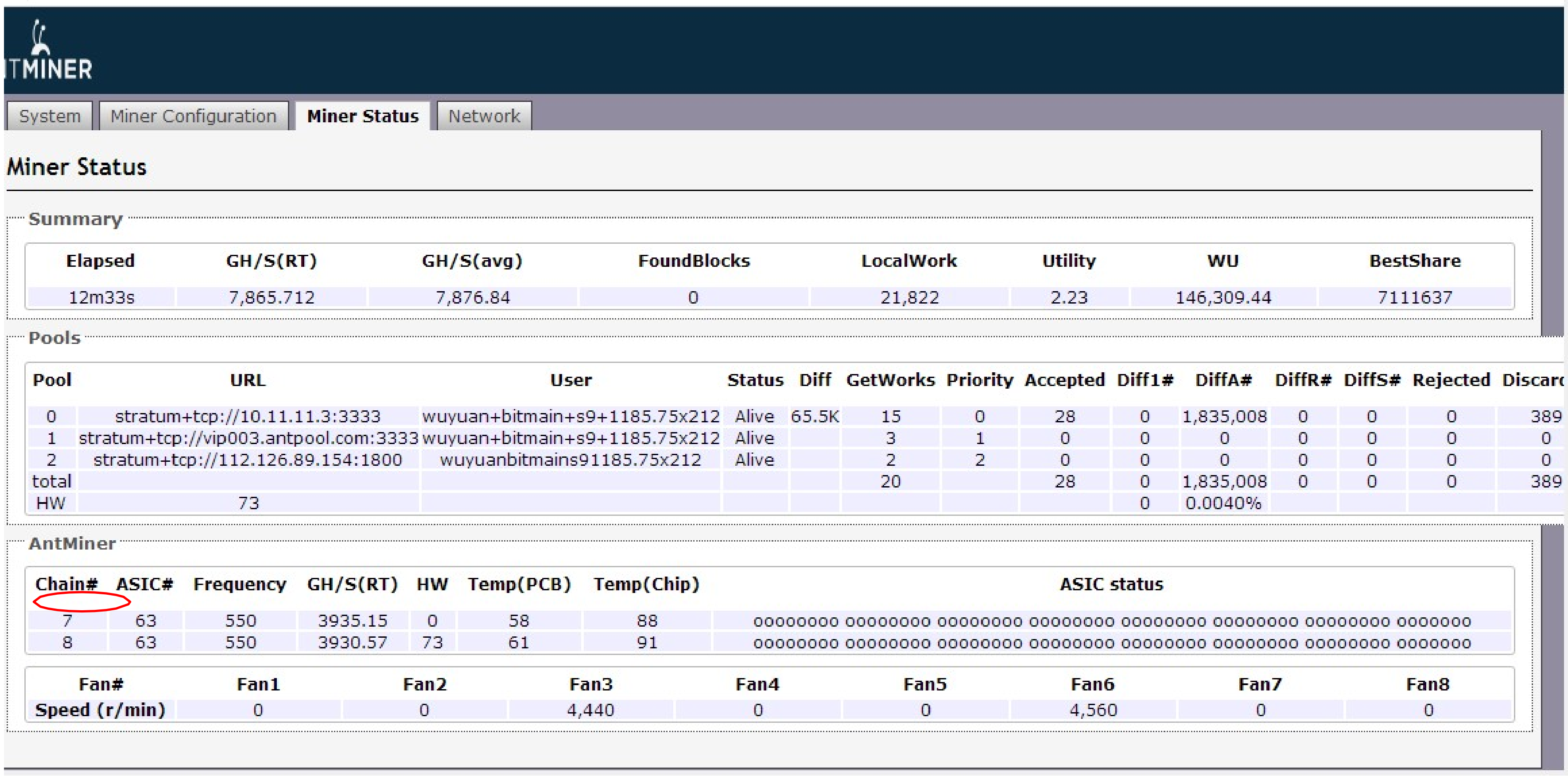
Fig 24. The Chip of Hashboard Drops



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
12m33s	7,865.712	7,876.84	0	21,822	2.23	146,309.44	7111637

Pools

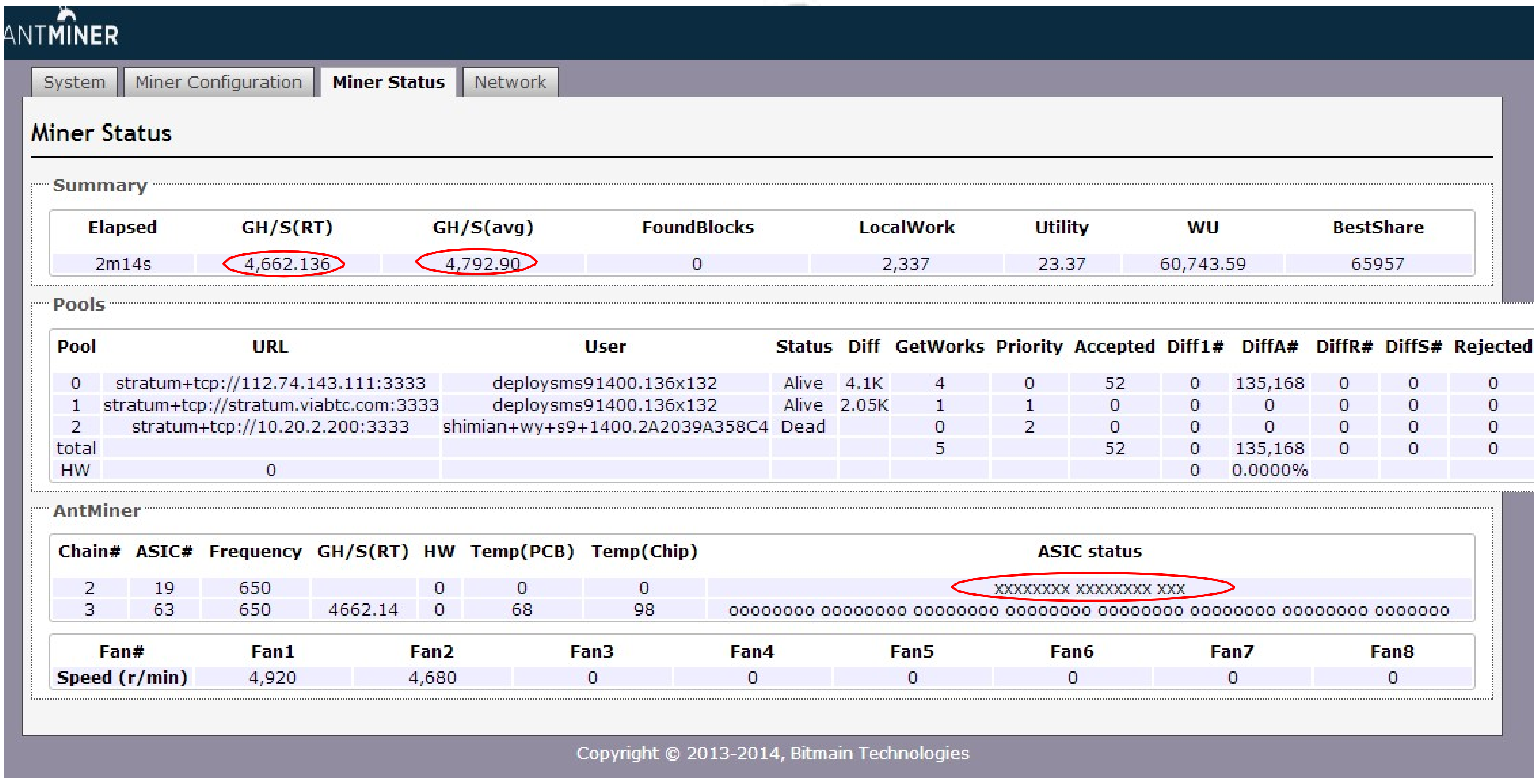
Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarc
0	stratum+tcp://10.11.11.3:3333	wuyuan+bitmain+s9+1185.75x212	Alive	65.5K	15	0	28	0	1,835,008	0	0	0	389
1	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.75x212	Alive		3	1	0	0	0	0	0	0	0
2	stratum+tcp://112.126.89.154:1800	wuyuanbitmains91185.75x212	Alive		2	2	0	0	0	0	0	0	0
total					20		28	0	1,835,008	0	0	0	389
HW	73							0	0.0040%				

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
7	63	550	3935.15	0	58	88	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
8	63	550	3930.57	73	61	91	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	4,440	0	0	4,560	0	0

Fig 25. Miner Losses One Hashboard



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
2m14s	4,662.136	4,792.90	0	2,337	23.37	60,743.59	65957

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected
0	stratum+tcp://112.74.143.111:3333	deploysms91400.136x132	Alive	4.1K	4	0	52	0	135,168	0	0	0
1	stratum+tcp://stratum.viabtc.com:3333	deploysms91400.136x132	Alive	2.05K	1	1	0	0	0	0	0	0
2	stratum+tcp://10.20.2.200:3333	shimian+wy+s9+1400.2A2039A358C4	Dead		0	2	0	0	0	0	0	0
total					5		52	0	135,168	0	0	0
HW	0							0	0.0000%			

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
2	19	650		0	0	0	xxxxxxxx xxxxxxxx xxx
3	63	650	4662.14	0	68	98	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	4,920	4,680	0	0	0	0	0	0

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Fig 26. Miner Losses Panel or Chip Appears X

Above phenomena are all caused by the fault of miner's hashboard. No. 8 hashboard in Fig 24 only finds 34 chips, so use tool to give single board test to No. 8 board, to find fault cause. Fig 25 cannot find No. 6 board, check the correspondence IO drop-out line, to see whether the power cord is connected well. If there is no problem, use tool to give single board test to No. 6 board; Fig 26 cannot find No. 1 board and No. 2 board has only 19 chips and cannot work, check No. 1 IO and power supply plug wire, and use tool to give single board test to No. 1 and No. 2 boards.

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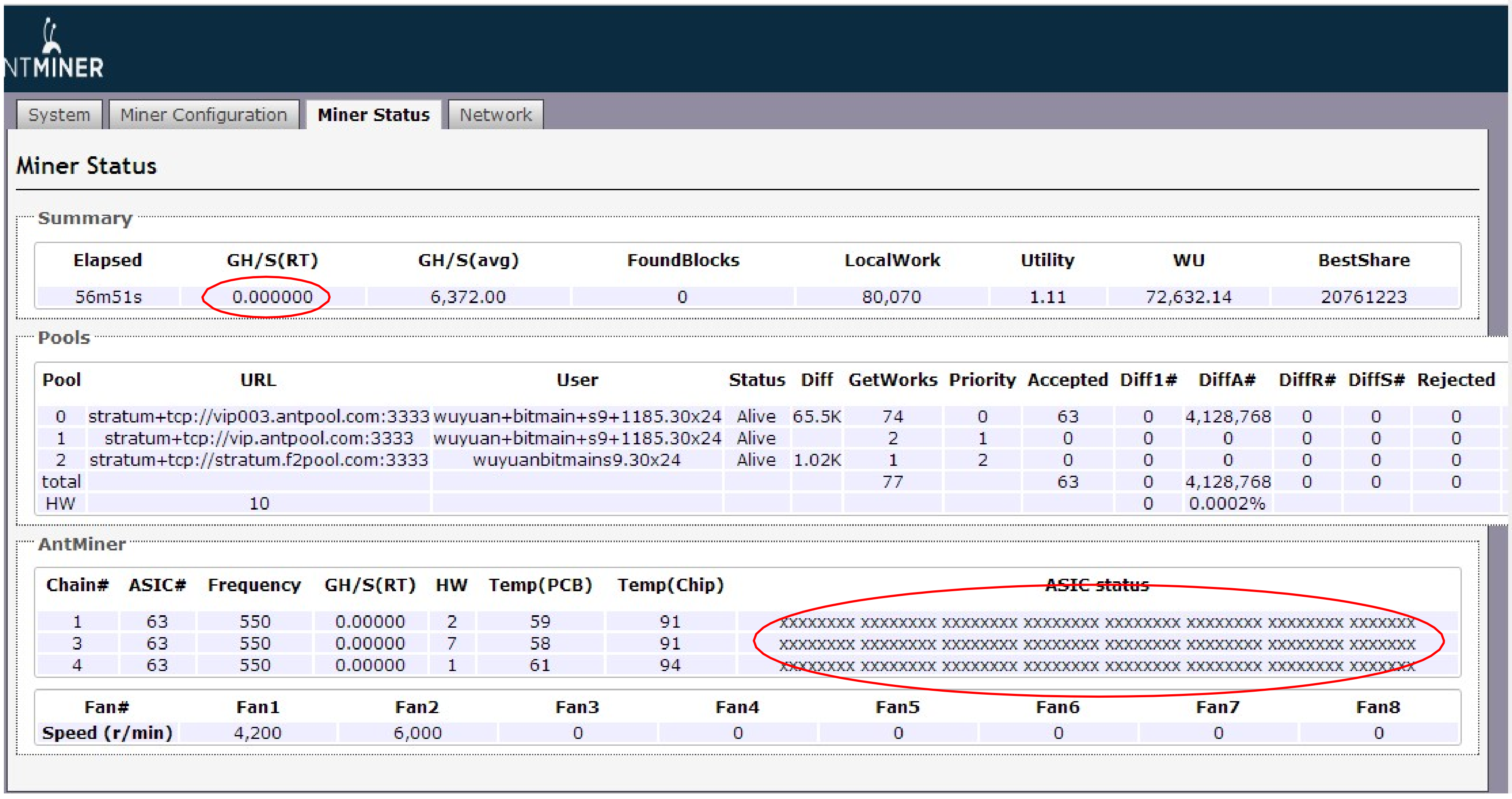
4) No GH/S(RT) hash rate, GH/S(AVG) hash rate drops, chip appears XX, and red light blinks. See Fig 27:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
56m51s	0.000000	6,372.00	0	80,070	1.11	72,632.14	20761223

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected
0	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.30x24	Alive	65.5K	74	0	63	0	4,128,768	0	0	0
1	stratum+tcp://vip.antpool.com:3333	wuyuan+bitmain+s9+1185.30x24	Alive		2	1	0	0	0	0	0	0
2	stratum+tcp://stratum.f2pool.com:3333	wuyuanbitmains9.30x24	Alive	1.02K	1	2	0	0	0	0	0	0
total					77		63	0	4,128,768	0	0	0
HW	10							0	0.0002%			

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Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
1	63	550	0.00000	2	59	91	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx
3	63	550	0.00000	7	58	91	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx
4	63	550	0.00000	1	61	94	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx

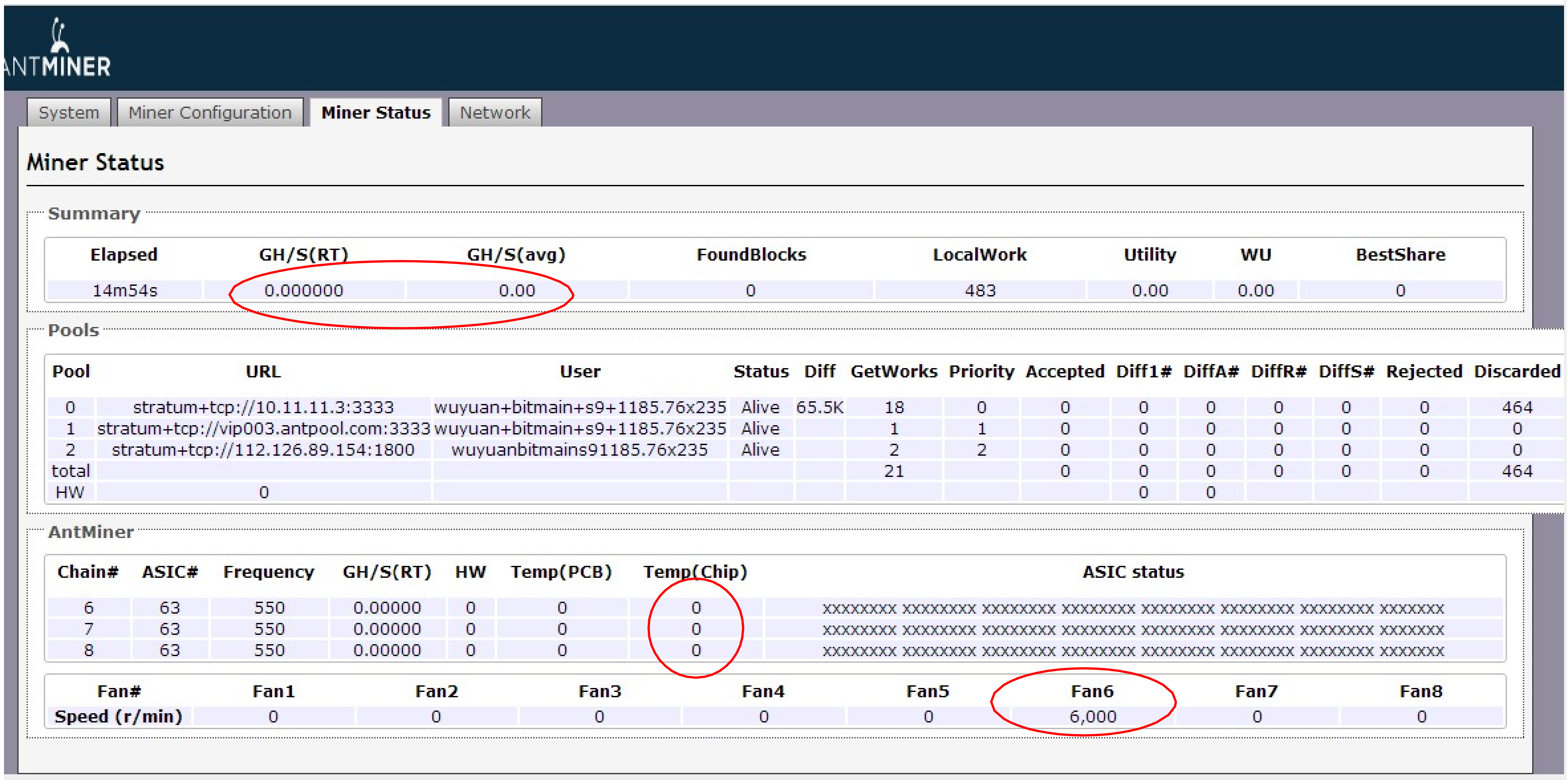
Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	4,200	6,000	0	0	0	0	0	0

Fig 27. All Chips Appear XX

The above phenomenon is that GH/S(RT) is 0, GH/S(AVG) hash rate drops, all chips appear XX, and red light blinks. This phenomenon is often caused by the operation anomaly of control panel due to that miner is disturbed. Please check the earthing of miner's shelf, socket, 220V power cord, AC-DC power supply, and the static electricity of environment.

If there is no static electricity problem and has proper earthing, upgrade latest firmware and use tool to give single board test to hashboard.

5) No GH/S(RT), no GH/S(AVG), and red light blinks. See Fig 28



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
14m54s	0.000000	0.00	0	483	0.00	0.00	0

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded
0	stratum+tcp://10.11.11.3:3333	wuyuan+bitmain+s9+1185.76x235	Alive	65.5K	18	0	0	0	0	0	0	0	464
1	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.76x235	Alive		1	1	0	0	0	0	0	0	0
2	stratum+tcp://112.126.89.154:1800	wuyuanbitmains91185.76x235	Alive		2	2	0	0	0	0	0	0	0
total					21		0	0	0	0	0	0	464
HW	0							0	0				

AntMiner

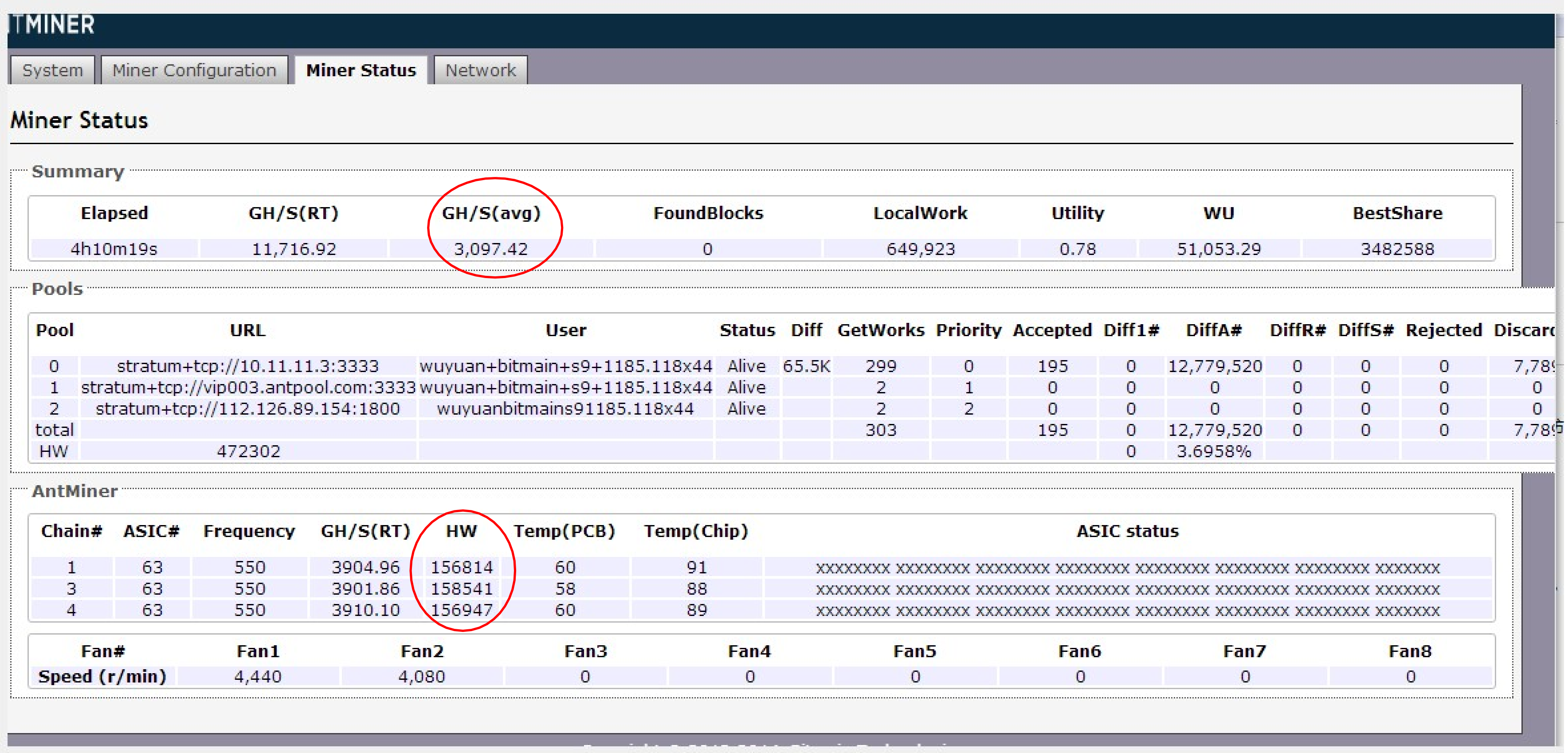
Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
6	63	550	0.00000	0	0	0	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx
7	63	550	0.00000	0	0	0	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx
8	63	550	0.00000	0	0	0	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	0	0	0	6,000	0	0

Fig 28. Only One Fan is Detected

In this phenomenon, there is not even temperature. As shown in above Fig, only one fan is detected. The reason is that miner only detects one fan and starts protection. Check the plug wires of the two fans or find a normal fan for replacement.

6) Has GH/S(RT), GH/S(AVG) is low, and all chips appear X. See Fig 29:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
4h10m19s	11,716.92	3,097.42	0	649,923	0.78	51,053.29	3482588

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discar
0	stratum+tcp://10.11.11.3:3333	wuyuan+bitmain+s9+1185.118x44	Alive	65.5K	299	0	195	0	12,779,520	0	0	0	7,78
1	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.118x44	Alive		2	1	0	0	0	0	0	0	0
2	stratum+tcp://112.126.89.154:1800	wuyuanbitmains91185.118x44	Alive		2	2	0	0	0	0	0	0	0
total					303		195	0	12,779,520	0	0	0	7,78
HW	472302							0	3.6958%				

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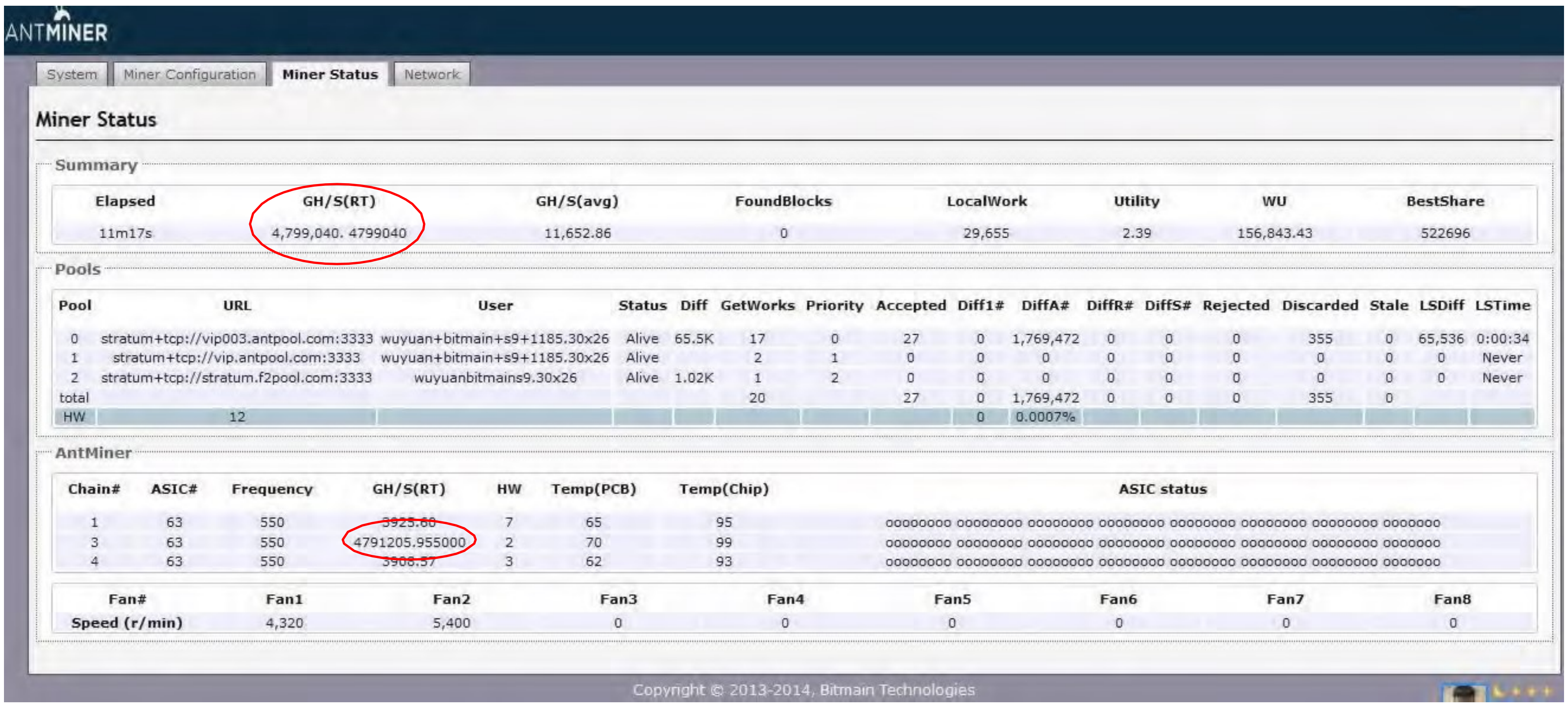
Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
1	63	550	3904.96	156814	60	91	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx
3	63	550	3901.86	158541	58	88	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx
4	63	550	3910.10	156947	60	89	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxx

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	4,440	4,080	0	0	0	0	0	0

Fig 29. GH/S(avg) Low Hasing and All Chips Appear X

In four hours of operation, HW reaches as much as 150,000. Under this phenomenon, use test tool to test every hashboard firstly. If there is no problem with hashboard, retain the configuration and upgrade to the latest firmware.

7) GH/S(RT) is extra high. See Fig 30:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
11m17s	4,799,040. 4799040	11,652.86	0	29,655	2.39	156,843.43	522696

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime
0	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.30x26	Alive	65.5K	17	0	27	0	1,769,472	0	0	0	355	0	65,536	0:00:34
1	stratum+tcp://vip.antpool.com:3333	wuyuan+bitmain+s9+1185.30x26	Alive		2	1	0	0	0	0	0	0	0	0	0	Never
2	stratum+tcp://stratum.f2pool.com:3333	wuyuanbitmains9.30x26	Alive	1.02K	1	2	0	0	0	0	0	0	0	0	0	Never
total					20		27	0	1,769,472	0	0	0	355	0		
HW	12							0	0.0007%							

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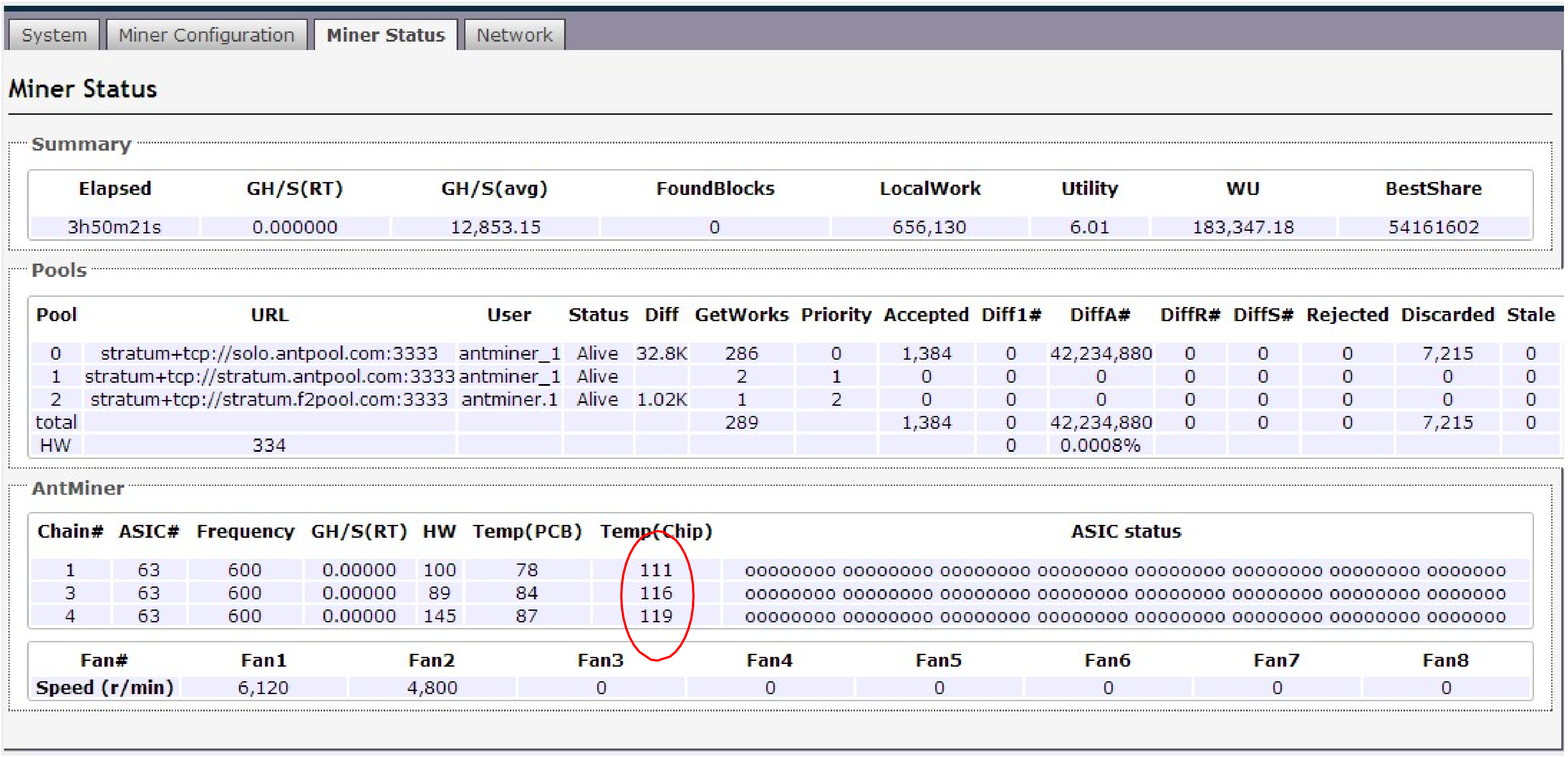
Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
1	63	550	3925.60	7	65	95	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
3	63	550	4791205.955000	2	70	99	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
4	63	550	3908.57	3	62	93	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	4,320	5,400	0	0	0	0	0	0

Fig 30. GH/S(RT) Extra High

It can be seen from above Fig: the hashing of No. 3 board reaches 4791T, this number is definitely wrong. Some wrong signals of No. 3 board cause the information that control panel receives is in disorder. Use test tool to give single board test to No. 3 hashboard. It is necessary to do a stress test, compare 550M hashboard, use 600M frequency test, and find the chip with low hashing for replacement.

8) No GH/S(RT) hashing, red light blinks and gives an alarm. See Fig 31:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
3h50m21s	0.000000	12,853.15	0	656,130	6.01	183,347.18	54161602

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale
0	stratum+tcp://solo.antpool.com:3333	antminer_1	Alive	32.8K	286	0	1,384	0	42,234,880	0	0	0	7,215	0
1	stratum+tcp://stratum.antpool.com:3333	antminer_1	Alive		2	1	0	0	0	0	0	0	0	0
2	stratum+tcp://stratum.f2pool.com:3333	antminer.1	Alive	1.02K	1	2	0	0	0	0	0	0	0	0
total					289		1,384	0	42,234,880	0	0	0	7,215	0
HW	334							0	0.0008%					

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
1	63	600	0.00000	100	78	111	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
3	63	600	0.00000	89	84	116	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo
4	63	600	0.00000	145	87	119	oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo oooooooo ooooooo

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	6,120	4,800	0	0	0	0	0	0

Fig 31. No GH/S(RT), Red Light Blinks, Gives an Alarm

Alarm phenomenon is usually caused by network anomaly, temperature anomaly, or fan anomaly. As shown in above Fig, the temperatures of the three boards have exceeded the upper limit of Temp (chip) and caused the alarm of protection. Check the air quantity of miner's air passage, to see whether the air passage is blocked, the fan is damaged, or there is dust between the teeth of cooling fin of hashboard.

2. Cannot log in monitoring interface (WEB), including cannot find miner or IP.

This phenomenon is mostly caused by the problem of control panel, especially firmware cause. Under this phenomenon, firstly perform factory reset, to see whether can log in background; if possible, upgrade firmware.

However, there are two types of control panels and the methods to factory reset are different.

One is C5 control panel (C5 control panel is composed of IO panel and BB panel), see Fig 32; and the other is **XILINX, belonging to all-in-one panel, see Fig 33.**

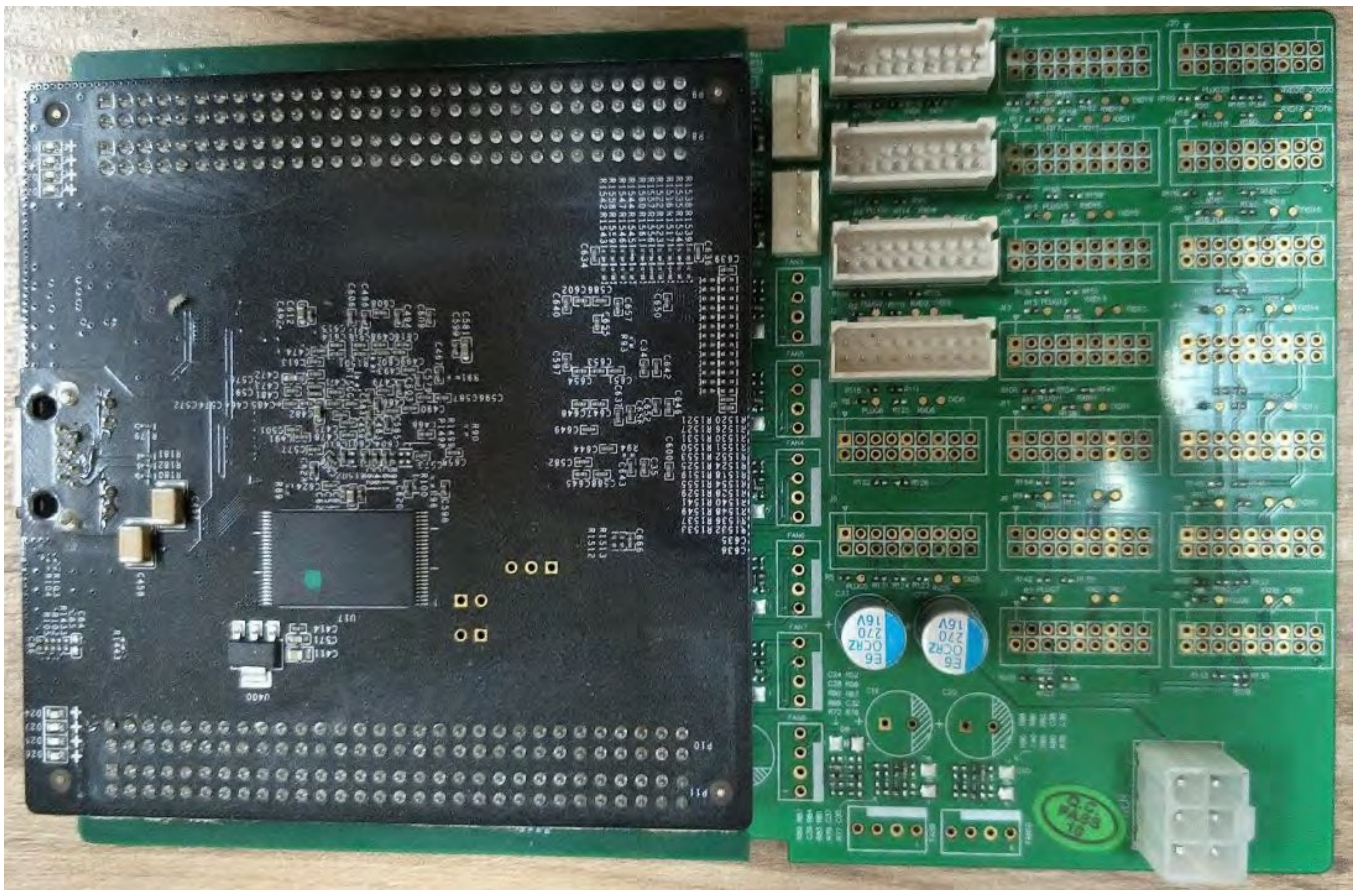


Fig 32. C5 Control Panel

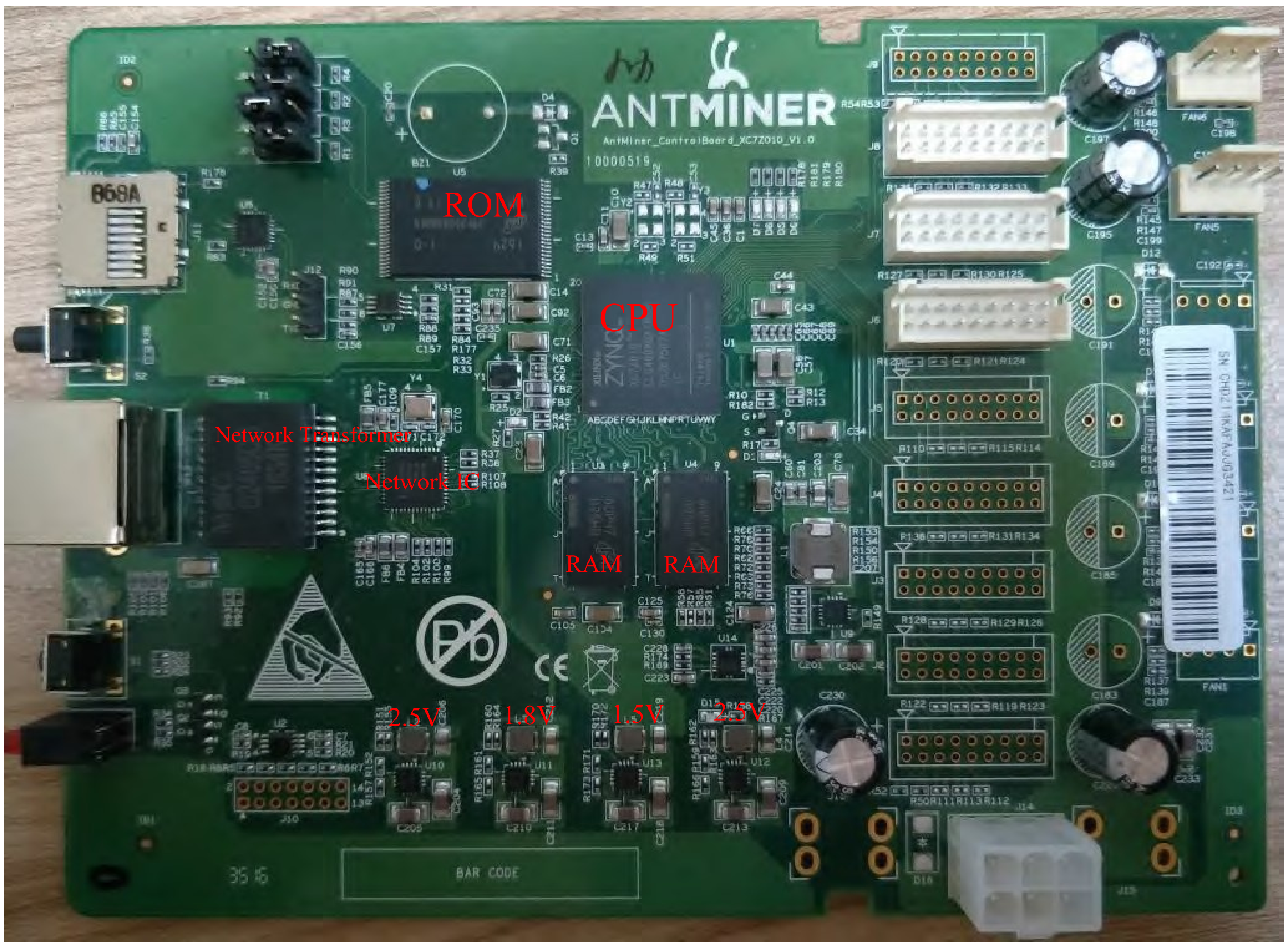

ROM
CPU
Network Transformer
Network IC
RAM
RAM
2.5V
1.8V
1.5V
2.5V

Fig 33. XILINX Control Panel

In the maintenance and repair of complete machine, the overall structure of control panel cannot be seen clearly. We can recognize them from appearances: for instance, the net light of C5 control panel is downward, as shown in below Fig 34; and the net light of XILINX control panel is upward, as shown in below Fig 35.

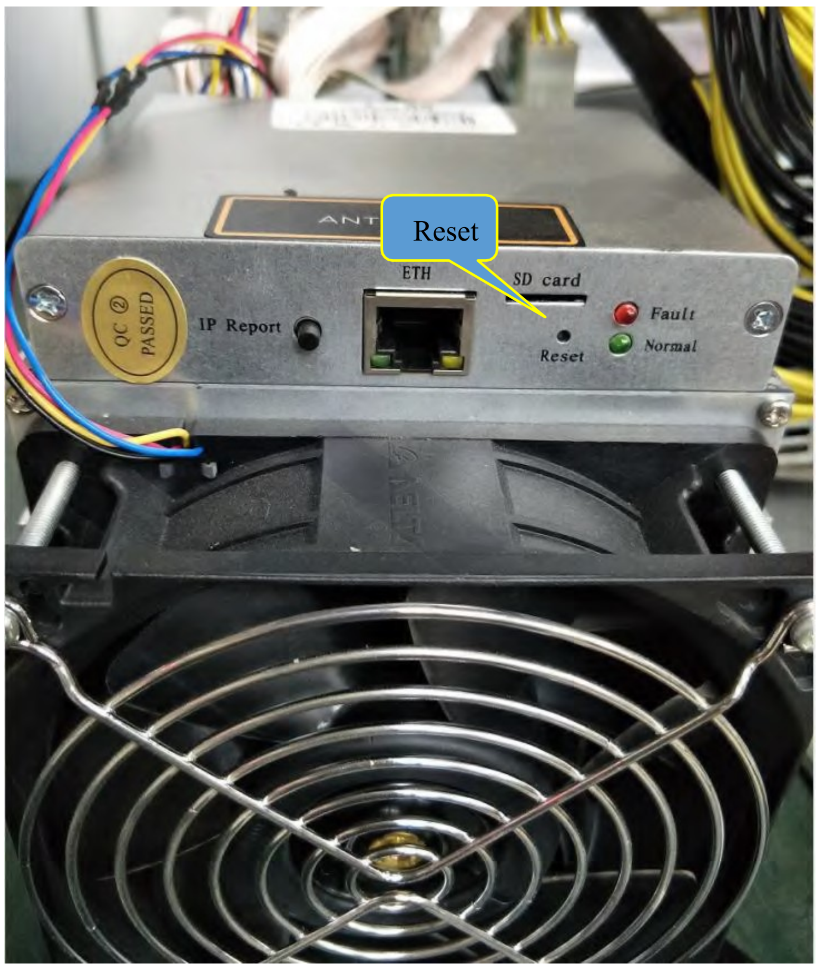

Reset
ETH
SD card
IP Report
Fault
Normal
Reset
QC ② PASSED

Fig 34. C5 Control Panel Appearance

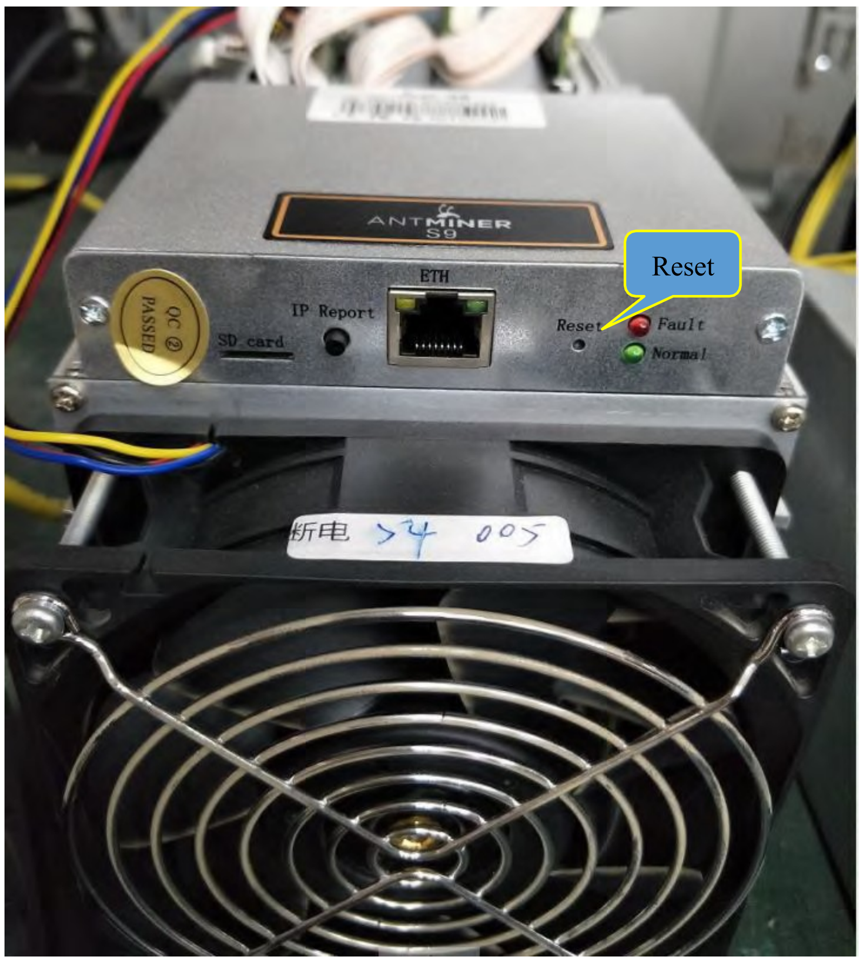
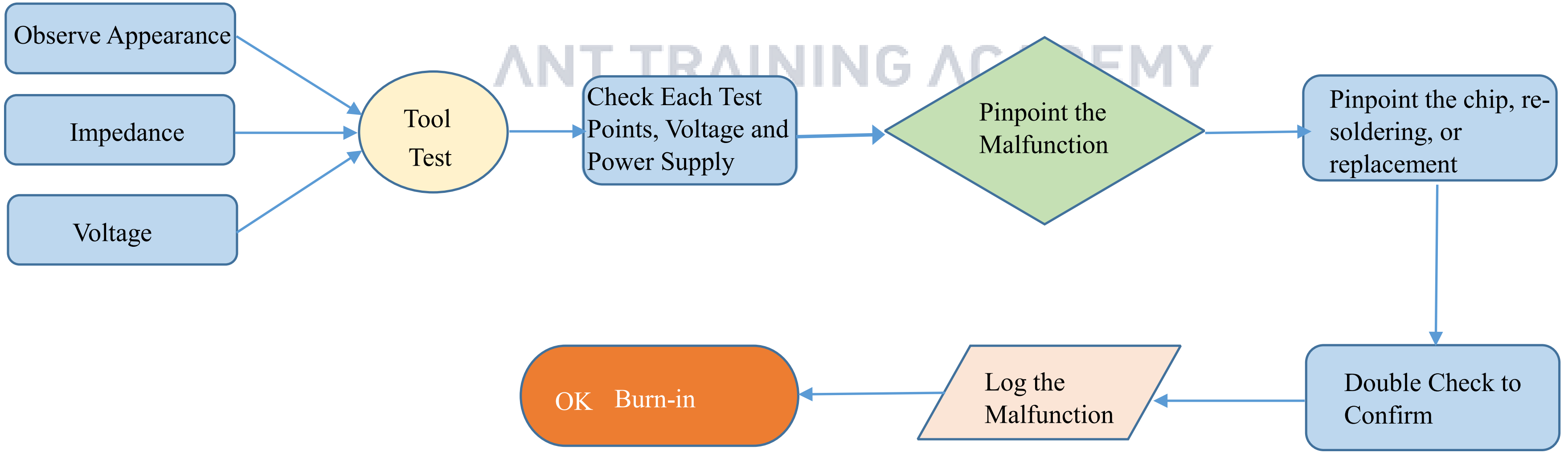

Reset
ANTMINER S9
ETH
IP Report
SD card
Reset
Fault
Normal
QC ② PASSED
断电 >4 005

Fig 35. XILINX Control Panel Appearance

Factory reset of C5 control panel: long press “RESET” key for more than 5 seconds after miner works; when the red light is on, reset miner successfully. Factory reset of XILINX control panel: In off mode, long press “IP Report” for more than 5 seconds and then let go, to complete factory reset. If factory reset has no effect, enter control panel maintenance process.

VI. Maintenance Process:

- Sample:


Observe Appearance
Impedance
Voltage
Tool Test
Check Each Test Points, Voltage and Power Supply
Pinpoint the Malfunction
Pinpoint the chip, re-soldering, or replacement
Double Check to Confirm
Log the Malfunction
OK Burn-in

1. Regular Check: Firstly, observe the target board to find cooling fin displacement, deformation or burn? Such issues take priority, displacement can be solved by taking it off, wash off the glue and re-glue it after the maintenance. Secondly, if there is no problem, then check impedance of each and every voltage domain to see if there is short/open circuit, which then takes priority. Thirdly, check if every domain reaches 0.4V and voltage different no greater than 0.05. Voltage too high or too low suggests anomalies in the neighboring domains. Check the causes.

2. After regular check (in which short circuit check is a must, in case of burning chips or other fittings when power is on), check the chip with hashboard tester, judge and pinpoint based on such result.

3. Based on hashboard tester results, check the voltages of test points (**CLK IN OUT/TX IN OUT/RX IN OUT/B IN OUT/RST IN OUT**), and **VDD VDD0V8 VDD1V8 VDD2V5** from the malfunctioning chip.

4. Signal flows, apart from RX (No.63 to No.1), are sequential (CLK CO BO RST) from No.1 to No.63. So, the anomaly can be identified with power sequence.

5. When pinpointing the malfunctioning chip, re-solder the chip: add scaling powder around the chip, heat the chip pin to dissolved state, move and press the chip lightly; have the chip pins and soldering pans re-grinded, finish. Note that if re-soldering does not help, the chip should be changed directly.

6. Run at least twice with hashboard tester on fixed hashboard. Test timing: first time should be after changing fittings, with cooled board. The second time should be in a few minutes with fully-cooled board. The gap between two tests will not affect working. Put aside the repaired board and continue with another one, come back to the first one with the fixed second one.

7. Log the malfunction type after maintenance, esp. the model, location and reason. This will further improve the feedback to production, CS and R&D.

8. Conduct formal burn-in after logging.

VII. ●Malfunction Types:

Typical malfunctions of **S9**:

1. Missing cooling fin or cooling fin displacement/deformation: No cooling fin displacement or touch on the **PCB** (back side of the board) before power-on, esp. fins in different voltages. Fins of different voltage domains touching will result in possible short circuits. Make sure all fins are in good condition of heat-transitioning and fixed tight.
Before replacing or re-implanting fins, clean the residue on the fin and the board first. Residue can be handled with anhydrous alcohol.

2. Imbalanced impedance among multiple voltage domains: When the impedance of certain domains is deviated from the norm, the anomaly domains could comprise open/short circuits. It is most likely that the chips are the cause. But there are 3 chips in each voltage domain; the problem could be with only one of them. Check and compare the earth impedance of each test point on chips to find the anomaly point and thus locating the problem chip.
Short Circuit: remove the cooling fin from the chips in the same voltage domain and observe chip pin to spot bridging issue.
If you cannot find short circuit point by observing, find it by resistivity method or interception method.

3. Imbalanced voltage among domains:

Voltage too high or too low suggests **IO** signal malfunction in the anomaly domain or the neighboring domain. This cause the next domain to show abnormal status and then voltage imbalance. Check the signals and voltages in test points to find the anomaly point. Some of the cases may require you to compare the impedance among multiple test points to find the anomaly.

Pay special attention: **CLK signal and RST signal — anomalies of these 2 are most frequently causing voltage imbalance.**

4. Missing chips: Missing chips means that when conducting hashboard tester checks, all **63** chips cannot be found, but only some of them. The actually missing (cannot find by checking) anomaly chips are not in the shown location. You need to pinpoint the anomaly chip by testing.

The pinpointing can be conducted by intercepting **TX**. Pivot the **TX** signal of a certain chip over the land, such as, after setting the **TX** output of chip No. **50**, over the earth and all previous chips are normal, the hashboard tester should show **50** chips. If not, the anomaly exists before No. **50**; if it does, the anomaly chip is after No. **50**. Repeat this until you locate the anomaly chip by dichotomy.

5. Broken link:

Broken links are similar to missing chips. The difference is that not all missing chips are in anomaly, but only one abnormal chip causing the following chips to fail. Such as, a certain chip is functional, but it does not transmit information from other chips; this signal chain will be broken right here — this is called broken link. Hashboard tester is capable of showing broken links. Such as when checking chips, hashboard tester reports only **14** chips; hashboard tester cannot start running until it detects pre-set number of chips, so it only shows the number of chips found. Based on the number "**14**", check the voltage and impedance at test points right before and after chip No. **14** will help you to locate the problem.

6. No running:

No running means the hashboard tester cannot detect the chip information of the hashboard and shows "**No hash board**"; this is the most frequent problem.

1) Voltage anomaly of a certain voltage domain: check the voltages among multiple domains to locate the problem.

2) Chip anomaly: Check signals among test points to locate the anomaly.

CLK signal: **0.9V**; signal is from chip No. **00** to No.**62**. But the current edition offers only 1 crystal oscillator, abnormal **CLK** causes all subsequent signals to show anomaly. Find the target in the sequence of signal transmission.

TX signal: **1.8V**; this signal is from chip No.**00**, **01**...**62**, look for previous ones when you hit anomaly at a certain point.

RX signal: **1.8V**; this signal return from **62**...**01**, **00**, identify the malfunction reason by checking signal direction. When no running happens to S7 and S9 board, this signal takes priority, check it first.

BO signal: **0V**; this signal means that when the chip detects RI return signal in a normal state, it can be lowered to low level, otherwise it should be high level.

RST signal: **1.8V**; when the board is powered on and **IO** signal is plugged in, this signal will transmit from **00**, **01**…**62** and till the last chip.

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3) Caused by a certain chip

Check the PD among multiple domains. In normal conditions, the **VDD** voltage is **0.4V**, all the voltages on other test points should be **0.4V** as well, a balance among multiple domains is necessary.

4) **VDD1V8** voltage anomaly of a certain chip

Check the test points of voltage domains to determine whether or not a certain **VDD1V8** is normal. Generally, **IO** voltage determines the voltage of test points. Therefore, when the **IO** voltage is **1.8V**, the test points have a normal voltage of **1.8V**.

5) **VDD2V5** anomaly of a certain chip
Make sure the voltage is normal. Abnormal voltage is related to low VDD voltage.

6) Buck and Booster Circuit Anomaly

Check the **C8 capacitor output** (up-left) and see if the voltage is between **8.27V and 9.07V.** Those who are not in the scope may be in need of a re-upgrade to the U3 PIC; make sure the PIC voltage is normal, check to see if U100 has an output of 14V; also check the un-checked peripheral parts and U100 per se.

7. Low hashing:

Low hashing can be divided into:
1) Hashboard tester shows **NG** due to insufficient **Nonce** and low hashing. The serial port shows information on the number of **Nence** each chip returns. Generally, if the **Nence** number is lower than the pre-set value, you should look for chip malfunction. If it is not due to poor soldering or peripheral reasons, you should just replace the chip.
2) Hashboard tester shows normal status, but after installation the hashing is low. This is generally due to poor cooling of the chips. Pay special attention to the cooling fin glue, and the general ventilation. Another reason could be that the voltage of a certain chip is critical, and after installation, the **12V** power supply is different from the test power supply, thus together resulting in a difference between test hashing and actual running hashing. Tune down and test with the hashboard tester, esp. with the **DC** adjustable **12V** power supply. Find the voltage domain that returns the minimum number of **Nence**.

8. NG of a certain chip:

Means that when test with hashboard tester, the port information shows the **Nence** is insufficient or zero of the return of a certain chip. If it's not due to poor soldering or peripheral reasons, just replace the chip.

VIII. ●Maintenance Notes:

1. The operator should be familiar with the function, flow direction, normal voltage and earth impedance values of each test point.
2. The operator should be familiar with chip soldering to avoid PCB blistering, deformation or pin damage.
3. BM1387 chip is packaged with 16 pins on both sides. Make sure of the polarity and coordinates when soldering.
4. When replacing chip, clean all the heat-conducting glue on the chip to avoid IC poor soldering or poor cooling (which causes second-time chip damage)

- Other Notes:

1. The Chip's back side cooling fins are earth connected with the chip, so it is imperative to use a long slim electro probe to check the test points. The probe should be fully insulated with heat-shrink tubes other than the metal on the tip to avoid that the probe touching the cooling fin and the test points at the same time. The voltage difference between upper and lower circuits, so touching the earth of different domains (cooling fins) and test points could cause man-made damage to the chip. Please pay special attention.
2. Soldering. There are cooling fins right next to the **PCB** on the back side of the chip, thus the cooling is fast. So during soldering, you would need auxiliary heating at the bottom (about **200** degrees Celsius). This improves efficiency and reduces damage to the PCB. Without auxiliary heating device, you need to remove the cooling fins on the **PCB** on the back side of the chip first before replacing the chip.

⚠ If there are any errors in this document, please contact writer to make corrections. We will keep analyzing and updating this content!

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